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REGISTERED TRADEMARK

ELECTRONICS I

Staff of Research and Education Association,
Dr. M. Fogiel, Director

This book covers the usual course outline of Electronics I. For more advanced topics, see *"THE ESSENTIALS OF ELECTRONICS II"*.

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WHAT "THE ESSENTIALS" WILL DO FOR YOU

This book is a review and study guide. It is comprehensive and it is concise.

It helps in preparing for exams, in doing homework, and remains a handy reference source at all times.

It condenses the vast amount of detail characteristic of the subject matter and summarizes the **essentials** of the field.

It will thus save hours of study and preparation time.

The book provides quick access to the important facts, principles, theorems, concepts, and equations of the field.

Materials needed for exams, can be reviewed in summary form – eliminating the need to read and re-read many pages of textbook and class notes. The summaries will even tend to bring detail to mind that had been previously read or noted.

This "ESSENTIALS" book has been carefully prepared by educators and professionals and was subsequently reviewed by another group of editors to assure accuracy and maximum usefulness.

Dr. Max Fogiel
Program Director

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CHAPTER 1

FUNDAMENTALS OF SEMICONDUCTOR DEVICES

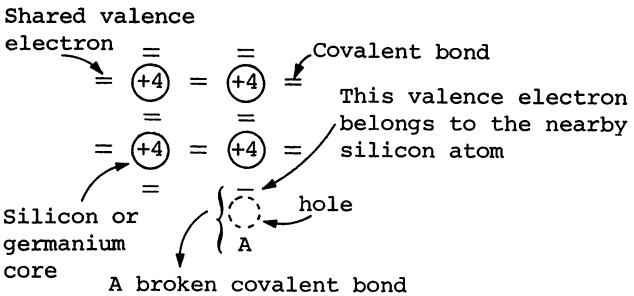
1.1 CHARGED PARTICLES AND THE ENERGY GAP CONCEPT

The electron:

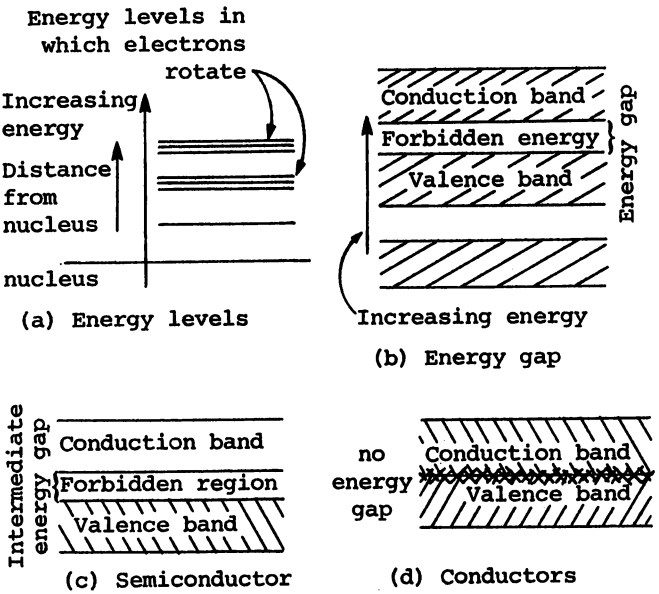
A) Negative charge = 1.60×10^{-19} coulomb

B) Mass = 9.11×10^{-31} kg

Hole - In a semiconductor, two electrons are shared by each pair of ionic neighbors through a covalent bond. When an electron is missing from this bond, it leaves a "hole" in the bond, creating a positive charge of 1.6×10^{-19}C.



The energy gap concept and classification of materials



Drift and the Diffusion Current:

A) The diffusion current - The movement of charged particles due to a non-uniform concentration gradient.

B) The drift current - The movement of charges under the influence of an electric field.

1.2 FIELD INTENSITY, POTENTIAL AND ENERGY

Potential - The work done against an electric field in taking a unit of positive charge from point A to B.

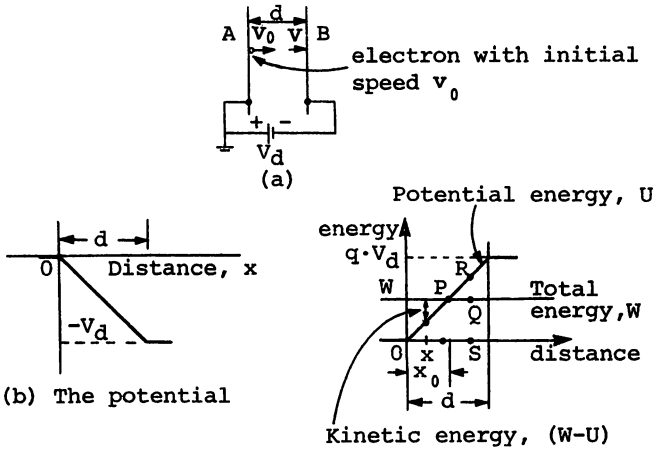
$$V = -\int_{x_0\ (\text{point A})}^{x\ (\text{point B})} E \cdot dx$$

Electric field intensity E:

$$E = \frac{-dv}{dx}$$

Potential energy U (in joules) equals the potential multiplied by the charge q.

Potential-energy barrier concept:



A) The kinetic energy is at its maximum when the electron leaves electrode A.

B) At P, no kinetic energy exists; the electron can therefore travel up to a distance x_0 from plate A.

The ev unit of energy: 1 ev = 1.60 $\times 10^{-19}$ J

1.3 MOBILITY AND CONDUCTIVITY

Mobility - When a metal is subjected to a constant E, a steady state is reached where the average value of the drift speed ν is attained. ν is proportional to E and is found by $\nu = \mu E$, where μ is the mobility of the electrons and

where the electric field has small values.

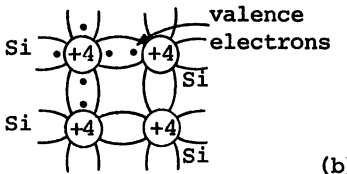
Current density: $J = \frac{I}{A} = \frac{N \cdot q \cdot \nu}{L\,A} = n \cdot q \cdot \nu = \rho \cdot \nu$

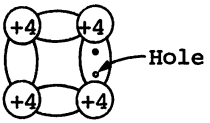
$\rho \equiv n \cdot q$ is the charge density; ν is the drift speed of the electrons.

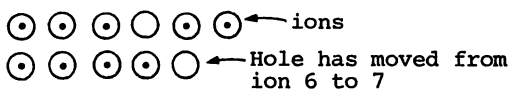
Conductivity: $J = nq \cdot \nu = n \cdot q \cdot \mu \cdot E$

$J = \sigma E$, where $\sigma = nq \cdot \mu$ = conductivity of the metal

1.4 ELECTRONS AND HOLES IN AN INTRINSIC SEMICONDUCTOR





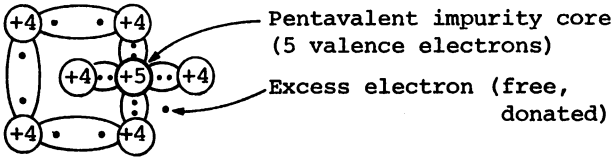


In an intrinsic semiconductor:

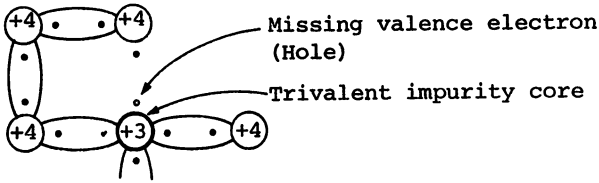
$n = p = n_i$ = density of the intrinsic carriers.

1.5 DONOR AND ACCEPTOR IMPURITIES

Donor impurity:



Acceptor impurity:



The mass-action law: $n \cdot p = n_i^2$

1.6 CHARGE DENSITIES IN A SEMICONDUCTOR

$N_D + p = N_A + n$, where N_D = positive charges contributed by the donor per meter^3, and N_A = negative charges contributed by the acceptor per meter^3.

$n \approx N_D$ (In an n-type material the free-electron concentration is equal to the density of the donor atoms.)

$p = \frac{n_i^2}{N_D}$ = Concentration of holes in the n type semiconductor

$p \approx N_A$ and $n = \frac{n_i^2}{N_A}$ (in a p-type material)

Generation and recombination of charges - On average, a hole or electron will exist for τ_p seconds or τ_n seconds, respectively, before recombination. This time interval is known as the "Mean Lifetime" of the hole or electron.

1.7 DIFFUSION AND THE POTENTIAL VARIATION WITHIN A GRADED SEMICONDUCTOR

Diffusion - The diffusion hole-current density J_p is, proportional to the concentration gradient.

$$J_p = -q \cdot D_p \cdot \frac{dp}{dx}$$

The Einstein relationship:

A) The Einstein equation: $\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = v_T$

(B) $V_T = \frac{KT}{q}$ = "Volt-equivalent of temperature"

$= \frac{T}{11,600}$ (T = temperature in °K)

C) At room temperature, $V_T = 0.0259V$ and $\mu = 38.6D$

Total current:

$$J_p = q \cdot \mu_p \cdot p \cdot E - q \cdot D_p \cdot \frac{dp}{dx}$$

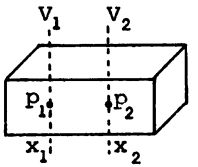
$$J_n = q \cdot \mu_n \cdot n \cdot E + q \cdot D_n \cdot \frac{dn}{dx}$$

The potential variation in a graded semiconductor:

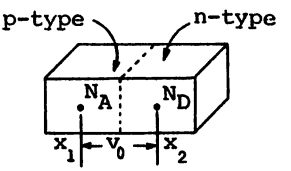
(A) $E = \frac{V_T}{p} \cdot \frac{dp}{dx}$ (E is the built-in field)

B) $E = \frac{-dv}{dx}$, hence $\boxed{dv = -V_T \cdot \frac{dp}{p}}$

C)



(a) A graded semiconductor, p(x) is not constant



(b) A step-graded jn

D) $V_{21} = V_2 - V_1 = V_T \cdot \ln \frac{p_1}{p_2}$

E) $\boxed{p_1 = p_2 \cdot e^{V_{21}/V_T}}$ This is the "Boltzmann relationship of kinetic gas theory".

F) Mass-action law: $n_1 = n_2 \cdot e^{-V_{21}/V_T}$ = Boltzmann equation for electrons

$n_1 p_1 = n_2 \cdot p_2$

G) An open-circuited, step-graded junction

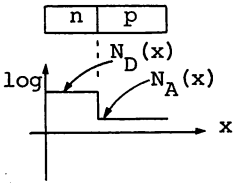
a) $V_0 = V_{21} = V_T \cdot \ln \frac{p_{p_0}}{p_{n_0}}$, $p_1 = p_{p_0}$ = thermal-equilibrium hole concentration in p-side and $p_2 = p_{n_0}$ = thermal-equilibrium hole in n-side

b) $p_{p_0} = N_A$ and $p_{n_0} = \frac{n_i^2}{N_D}$, such that

$$\boxed{V_0 = V_T \cdot \ln\left[\frac{N_A \cdot N_D}{n_i^2}\right]}$$

H) Analysis of p-n junction in thermal equilibrium.

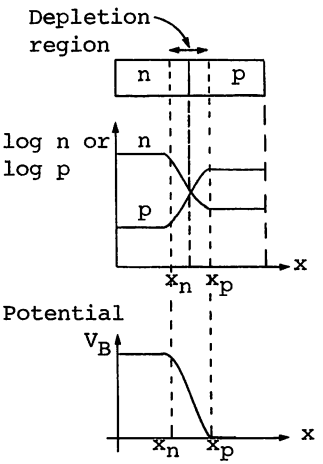
Approximate doping profile for a p-n step junction:



I) Unbiased p-n junction:

The equilibrium carrier concentration and potential as a function of distance in a p-n junction:

a) The region $x_n < x < x_p$ is called the "space-charge region" or "depletion region".



(a) Equilibrium carrier construction and potential

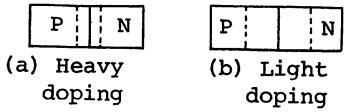
b) $$V_B = \text{built-in-voltage} = \frac{K \cdot T}{q} [\ln n_n - \ln n_p]$$

where

n_n = Electron concentration on n-side

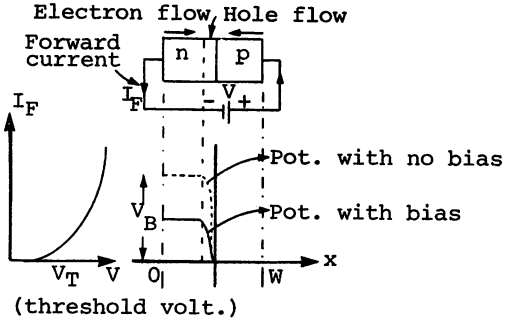
n_p = Electron concentration on p-side

Depletion region width:



(a) Heavy doping (b) Light doping

J) Forward bias junction



The potential distribution in a p-n junction

n_w (electron concentration at x = w) = $n_{p0} = n_i^2/N_A$

n_{p_0} = Equilibrium electron concentration in p-region

x = 0 is the right-hand edge of the depletion region

n_A = Acceptor concentration

n_T = Electron concentration at x = 0

$$n_T = n_n \exp\left\{\frac{-q(V_B - V)}{KT}\right\}$$

$n_T = n_{p_0} \exp\left[\frac{q \cdot V}{KT}\right]$, n_{p_0} = electron concentration

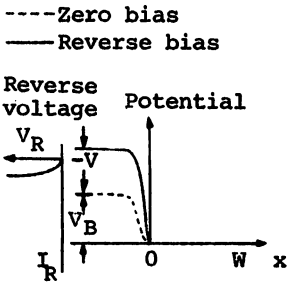
Current density: $J_e = q \cdot D_e \cdot \frac{dn}{dx} = q \cdot D_e \frac{(n_w - n_T)}{w}$

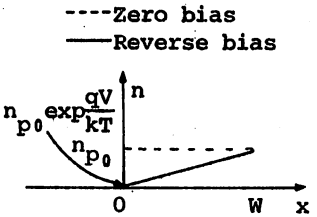
$$= -q \cdot \frac{D_e n_i^2}{N_A w}\left(\exp\left[\frac{qv}{KT}\right] - 1\right)$$

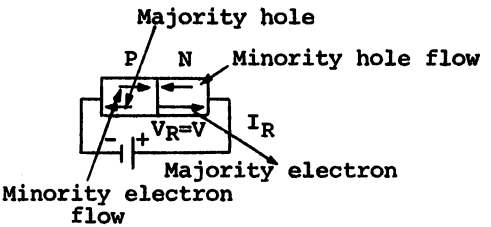
The hole current is small compared to the electron current.

Reverse bias:

The potential distribution and electron concentration profile:







The total current flowing into the p-regin is:

$$I = I_s(\exp\frac{q \cdot v}{KT} - 1) \quad \text{where } I_s = \frac{q \cdot D_e \cdot n_i^2 \cdot A}{w \cdot N_A}$$

CHAPTER 2

JUNCTION DIODE: THEORY AND SIMPLE CIRCUIT ANALYSIS

2.1 THE OPEN-CIRCUITED P-N JUNCTION

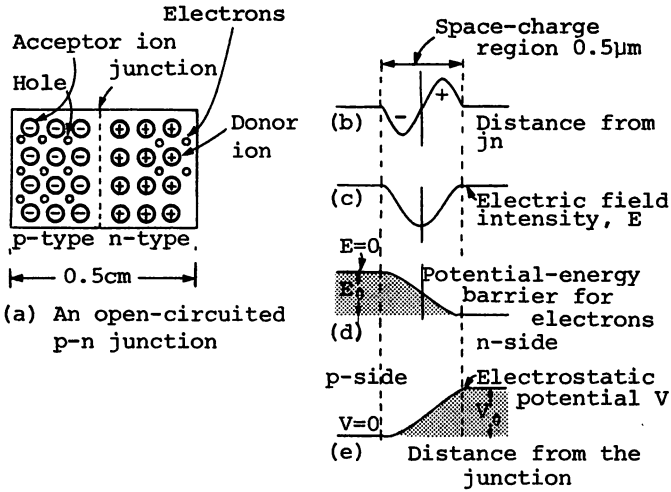


Fig. 1 A schematic diagram of a p-n junction. Since potential energy = potential x charge, the curve in (d) is proportional to the energy for a hole & curve in (e) is proportional to the -ve of that in (d). (It is assumed that the diode dimensions are large compared with the space charge region.)

2.2 THE P-N JUNCTION AS A RECTIFIER

Reverse bias - The polarity is such that it causes both the holes in p-type and the electrons in n-type to move away from the junction. This cannot continue for long because the holes must be supplied across the junction from the n-type material.

A zero current would result, except that thermal energy present will create a small current, known as the "reverse saturation current," I_0. This current increases with increasing temperature.

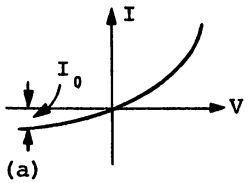
Forward bias - In this case, the resultant current crossing the junction is the sum of the hole and the electron minority currents.

2.3 V-I CHARACTERISTICS

For a p-n junction, $I = I_0(e^{V/\eta \cdot V_T} - 1)$,

$V_T = \frac{T}{11600}$ = Volt-equivalent of temperature

The characteristics:



The reverse-bias voltage V_R is the voltage below which the current is very small (<1% of the maximum rated value).

2.3.1 TEMPERATURE DEPENDENCE OF THE V-I CHARACTERISTICS

$$I_0(T) = I_{01} \times 2^{(T-T_1)/10} \quad (I_0 = I_{01} \text{ at } T = T_1)$$

$$\boxed{\frac{dV}{dT} \approx -2.5 \text{ mv/°C}}$$

2.4 DIODE RESISTANCE, TRANSITION AND DIFFUSION CAPACITANCE

Diode resistance:

The static resistance R is the ratio V/I.

For a small-signal operation, the "Dynamic-resistance" r is:

$$r \equiv \frac{dV}{dI} \text{ (depending on the oeprating voltage)}$$

$$g = \frac{1}{r} = \frac{dI}{dV}$$

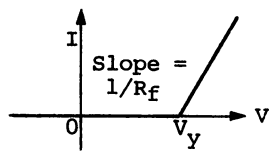
$$= I_0 \frac{\exp\left[\frac{V}{\eta V_T}\right]}{\eta V_T}$$

$$= (I + I_0)/\eta \cdot V_T$$

For $I \gg I_0$,

$$\boxed{\gamma \approx \frac{\eta \cdot V_T}{I}}$$

Piecewise linear characterization of a semiconductor diode



The break-point is not at the origin but at a point V_y units from the origin. V_y is called the offset voltage.

R_f is the forward resistance.

Transition and diffusion capacitance:

In the reverse bias region, the transition capacitance predominates, while in the forward bias region, the diffusion or storage capacitance predominates.

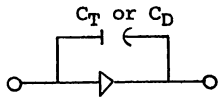
Transition capacitance, C_T:

$$C_T = \left| \frac{dQ}{dV} \right|$$

Note: C_T depends on the magnitude of the reverse voltage, since the magnitude of the reverse voltage determines the depletion width.

Diffusion capacitance, C_D:

C_D is introduced when the p-n junction is forward biased due to the additional injected charge redistribution in the n-region.



This type of capacitance limits switching speed in logic circuits used as junction devices.

Static derivation of C_D:

$$C_D = \frac{dQ}{dV} = \tau \cdot \frac{dI}{dV} = \tau \cdot g = \frac{\tau}{r}$$

$$C_D = \frac{\tau \cdot I}{\eta \cdot V_T}$$

For reverse bias, g is very small and $C_D << C_T$.

For a forward current, $C_D >> C_T$.

$$r \cdot C_D = \tau$$

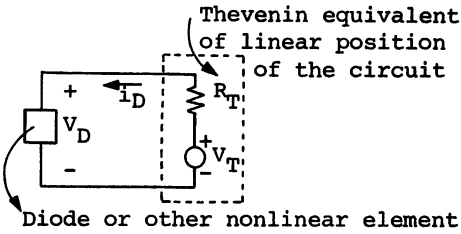
The diode time constant equals the mean lifetime of minority carriers.

2.5 ANALYSIS OF SIMPLE DIODE CIRCUITS: CONCEPT OF DYNAMIC RESISTANCE AND A.C. LOAD LINE

2.5.1 THE D.C. LOAD LINE

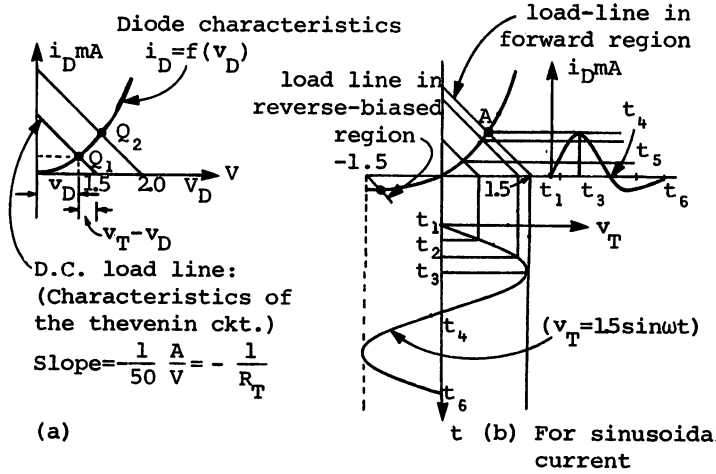
The behavior of the diode at low frequency is marked by V-I characteristics.

Other elements of a circuit beyond the region bounded by the diode and its terminals can be replaced by a thevenin equivalent circuit.



For the non-linear element $i_D = f(v_0)$, the thevenin equivalent is given as $v_D = v_T - i_D \cdot R_T$.

The problem is solved by plotting these equations on the same set of axes.



The straight-line characteristics of the thevenin circuit is "D.C. load line." As long as R_T remains constant, any change in v_T is accounted for by a horizontal shift of the load line.

If v_T is sinusoidal, the corresponding current i_D can be found as shown in (b).

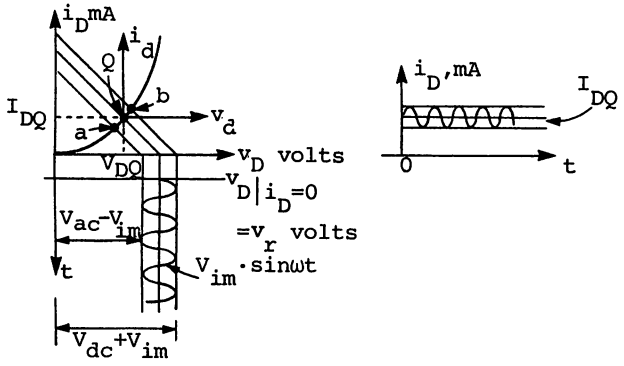
Small-signal analysis, dynamic resistance:

Small-signal - When the total peak-to-peak swing of the signal is a small fraction of its D.C. component.

$v_T = V_{dc} + v_i = V_{dc} + V_{im} \sin \omega t$

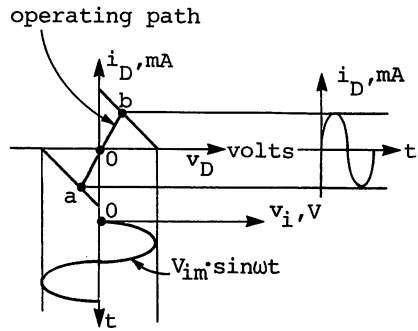
(where V_{dc} = bias voltage, and $V_{im} << V_{Dc}$).

The operating point for $v_T = V_{dc}$ is called "the quiescent point". It is found as follows:



A new set of axes i_d - v_D is constructed at Q (as shown below);

$$i_d = i_D - I_{DQ},\ v_d = v_D - V_{DQ}$$

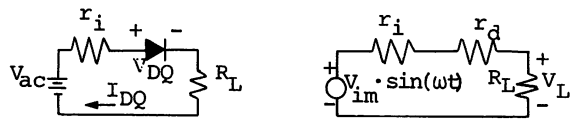


The operating path is "ab". The dynamic resistance r_d of the diode is equal to the inverse of the slope of line "ab".

$$r_d = \text{dynamic resistance} = \left.\frac{\Delta v_D}{i_D}\right|_{Q\ pt.}$$

If r_d is found, circuit variables are obtained by using Ohm's law.

The original circuit has two parts:



(a) For calculating Q

(b) For calculating small-signal a.c. component

Calculation of r_d:

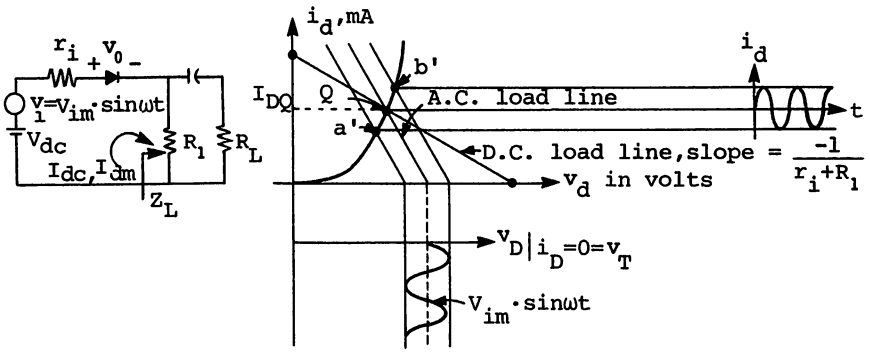
$$r_d = \left.\frac{dv_d}{di_D}\right|_{Q\ point} \cong \frac{V_T}{I_{DQ}} = \frac{2SmV}{I_{DQ}} \text{ (at T=300°K)}$$

Reactive elements:

$$I_{dm} = \text{(the peak current)} = V_{im} / |r_i + r_d + z_i|$$

2.5.2 THE A.C. LOAD LINE

For the circuit shown below, the D.C. load line and Q point are:



When the A.C. signal is present, the effective resistance seen by the diode is $r_i + (R_1 \| R_L)$. The A.C. load line is drawn through Q with slope = $\frac{-1}{[r_i + (R_1 \| R_L)]}$

The equations for the D.C. and A.C. load lines are:

$V_{dc} = I_{DQ}(r_i + R_1) + V_{DQ}$ D.C. load line

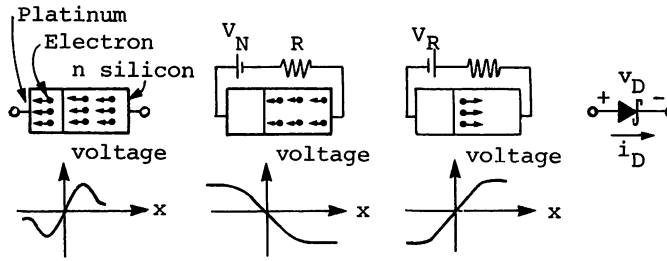
$v_i = i_d(r_i + [R_1 \| R_L]) + r_d$ A.C. load line

2.6 SCHOTTKY AND ZENER DIODES

Schottky diode:

It is formed by bonding a metal (platinum) to n-type silicon. A Schottky diode has negligible charge storage and is often used in high-speed switching applications.

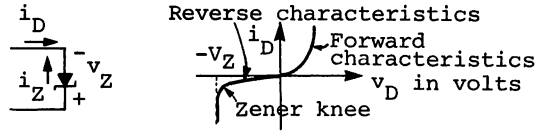
Platinum acts as an acceptor material for electrons when bonded to n-type silicon.



(a) Potential distribution after initial diffusion

(b) After application of a +ve voltage

Zener diode:



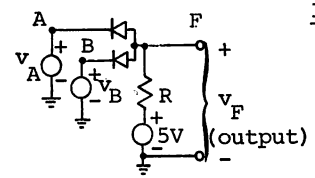
Unlike regular diodes, when you apply a high, reverse voltage across a Zener diode, you produce an almost constant-voltage region on the characteristic curve of the diode. One application of this special property of the Zener diode is voltage regulation.

The change of the Zener voltage V_Z as a result of a change of temperature is proportional to the Zener voltage as well as change in temperature.

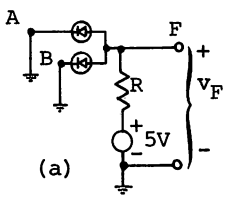
$$T_c = \text{Temperature coefficient} = \frac{\Delta V_Z / V_Z}{\Delta T} \times 100\%/^{\circ}C$$

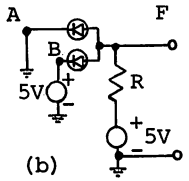
2.7 DIODE LOGIC CIRCUITS

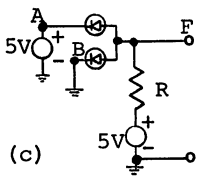
2.7.1 A DIODE "AND" GATE

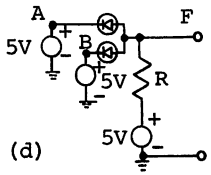


Inputs		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1



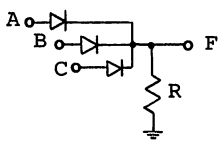






The diode AND gate redrawn for each possible combination of inputs. The diodes are assumed to be perfect rectifiers.

2.7.2 A DIODE "OR" GATE



(a)

Inputs			Output
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(b)

A diode OR gate. (a) The circuit. (b) The truth table. The output is 1 if any of the inputs is 1.

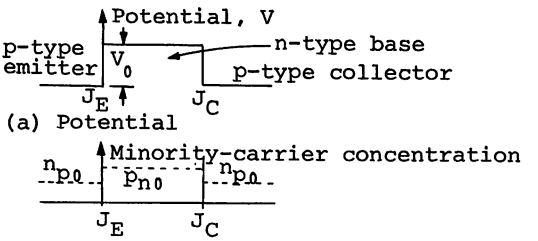
CHAPTER 3

THE BIPOLAR JUNCTION TRANSISTOR

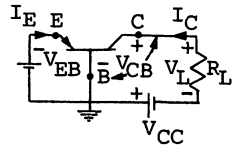
3.1 THE JUNCTION TRANSISTOR THEORY

3.1.1 OPEN-CIRCUITED TRANSISTOR

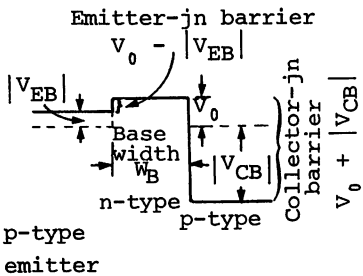
Under this condition, the minority concentration is constant within each section and is equal to its thermal-equilibrium value n_{p0} in p region and p_{n0} in n region. The potential barriers at the junctions adjust to the contact difference of potential V_0, such that no free carriers cross a junction.



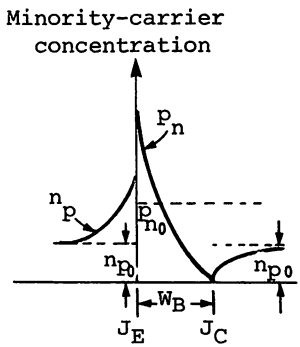
3.1.2 TRANSISTOR BIASED IN THE ACTIVE REGION



(a) p-n-p transistor biased in the active region.



(b) Potential variation through the transistor.



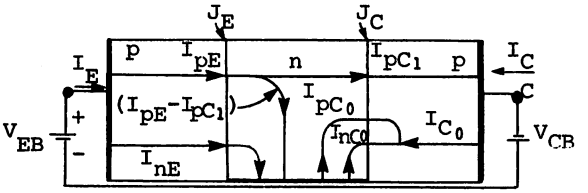
(c) Minority-carrier concentration

The dashed curve applies to the case before the application of external biasing voltages.

The forward biasing of the emitter junction lowers the emitter-base potential barrier by $|V_{EB}|$, permitting minority-carrier injection. Holes are thus injected into the base and electrons into the emitter region.

Excess holes diffuse across the n-type base, the holes which reach J_C fall down the potential barrier and are collected at the collector.

3.1.3 TRANSISTOR CURRENT COMPONENTS



Transistor current compoments for a forward-biased emitter junction and a reverse-biased collector junction.

I_{pE} - Current due to holes crossing from emitter into base is the forward injection.

I_{nE} - Electrons crossing from base into the emitter.

$I_E = I_{pE} + I_{nE}$ (I_{pE} has a magnitude proportional to the slope at J_E of the p_n curve. Similarly, I_{nE} has a magnitude proportional to the slope at J_E of the n_p curve.)

$-I_{co} = I_{nco} + I_{pco}$ (I_{nco} consists of electrons moving from the p to the n region across J_c, and I_{pco} results from holes across J_c from n to p.)

I_c = Complete collector current = $I_{co} - I_{pc}$

$$I_c = I_{co} - \alpha \cdot I_E$$

Large-signal current gain α: This is the ratio of the negative of the collector-current increment from cutoff ($I_c = I_{co}$), to the emiiter-current change from cutoff ($I_E = 0$), e.g.,

$$\alpha = \frac{-(I_c - I_{co})}{I_E - 0}$$

The large-signal current gain of a C-B transistor.

α is not a constant, but vaires with emitter current I_E, V_{CB} and temperature.

A generalized transistor equation gives an expression for I_c in terms of any V_c and I_E:

$$I_c = -\alpha I_E + I_{co}(1 - e^{V_c/V_T})$$

A transistor as an amplifier, and parameter α':

A small voltage change ΔV_i between emitter and base causes a relatively large emitter-current change

$$\Delta I_E \cdot \Delta I_c = \alpha' \cdot \Delta I_E, \quad \Delta V_L = -R_L \Delta I_c = -\alpha' \cdot R_L \cdot \Delta I_E.$$

If the dynamic resistance of the emitter junction is r_e, then

$$\Delta V_i = r_e \cdot \Delta I_E, \text{ and } A = \alpha' \cdot R_L (\Delta I_E / r_e) \Delta I_E = \frac{-\alpha' \cdot R_L}{r_e}$$

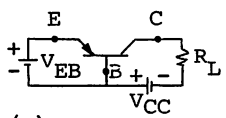
The parameter α':

α' = The negative of the small-signal Short-circuit current transfer ratio $\equiv \left.\frac{\Delta I_c}{\Delta I_E}\right|_{V_{CB}}$

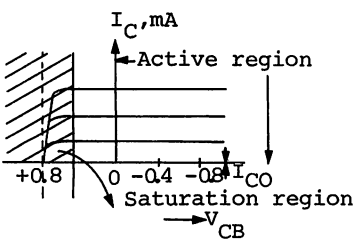
$\alpha' = -\alpha$ (assuming α is independent of I_E)

3.1.4 TRANSISTOR CONFIGURATION

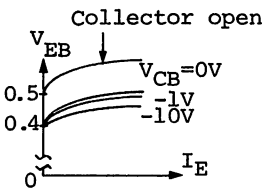
The CB configuration:



(a)

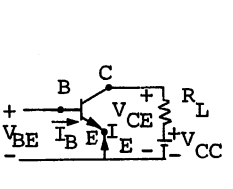


(b) Output characteristics

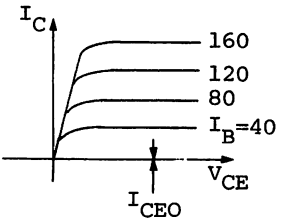


(c) Input characteristics

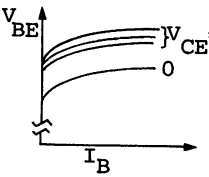
The common-emitter configuration:



(a)



(b) Output characteristics



(c) Input characteristics

$$I_c = \frac{I_{co}}{1-\alpha} + \frac{\alpha \cdot I_B}{1-\alpha}$$

$$\beta = \frac{\alpha}{1-\alpha}, \quad I_c = (1+\beta)I_{co} + \beta \cdot I_B$$

CE cutoff currents - A transistor is in cutoff if $I_E = 0$ and $I_c = I_{co}$. It is not in cutoff if the base is open-circuited.

Common-emitter current gain:

Large-signal current-gain $\beta = \dfrac{I_c - I_{CBo}}{I_B - (-I_{CBo})}$

DC current gain $h_{FE} = \beta_{dc} = \dfrac{I_C}{I_B}$

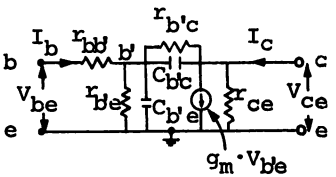
Small-signal current gain $h_{fe} = \beta' = \left.\dfrac{\Delta I_c}{\Delta I_B}\right|_{V_{CE}}$

3.2 THE JUNCTION TRANSISTOR: SMALL-SIGNAL MODELS

3.2.1 THE HYBRID-Pi MODEL

It is useful to predict high-frequency performance.

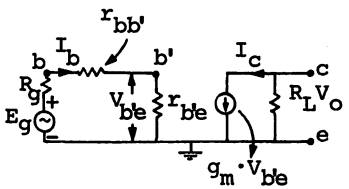
Model:



b,e,c: external terminals

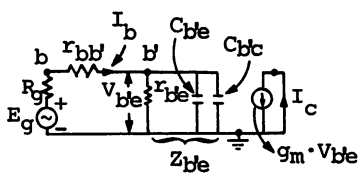
$C_{b'c}$ is the depletion-region capacitance of the collector-base junction. C_{be} is an equivalent capacitance that accounts for a reduction in gain and in increase in phase shift at higher frequency.

Simplified circuit valid at low frequencies:



$\frac{V_0}{V_{b'e}} = -g_m \cdot R_L$ (which is equivalent to A_v if $r_{bb'} << r_{b'e}$)

Beta cutoff frequency f_β : At this frequency the magnitude of h_{fe} has decreased 3dB from its mid-frequency value.



$$h_{fe} = \frac{I_c}{I_b} = \frac{g_m \cdot r_{be}}{1 + j\omega/\omega\beta}$$

$$\omega_\beta = 1/r_{b'e}(c_{b'e} + c_{b'c})$$

$$f_\beta = \frac{1}{2\pi \cdot r_{b'e} \cdot c_{b'e}} \quad \text{(since } c_{b'e} >> c_{b'c}\text{)}$$

$$f_T = h_{fe} \cdot f_\beta = \frac{g_m}{2\pi \cdot c_{b'e}}$$

3.2.2 h-PARAMETERS

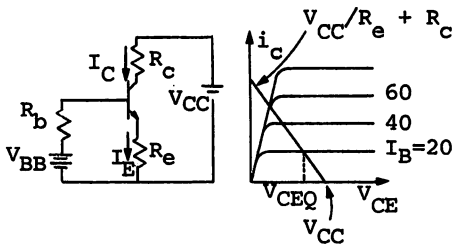
h-Parameters for Each Transistor Configuration in Terms of the Other Two.

		Common base	Common collector
Common emitter	h_{ie}	$\frac{h_{ib}}{h_{fb} + 1}$	h_{ic}
	h_{fe}	$-\frac{h_{fb}}{h_{fb} + 1}$	$-(h_{fc} + 1)$
	h_{oe}	$\frac{h_{ob}}{h_{fb} + 1}$	h_{oc}
	h_{re}	$\frac{h_{ib}h_{ob}}{1 + h_{fb}} - h_{rb}$	$1 - h_{rc}$
		Common emitter	**Common collector**
Common base	h_{ib}	$\frac{h_{ie}}{h_{fe} + 1}$	$-\frac{h_{ic}}{h_{fc}}$
	h_{fb}	$\frac{-h_{fe}}{h_{fe} + 1}$	$-\frac{h_{fc} + 1}{h_{fc}}$
	h_{ob}	$\frac{h_{oe}}{h_{fe} + 1}$	$-\frac{h_{oc}}{h_{fc}}$
	h_{rb}	$\frac{h_{ie}h_{oe}}{h_{fe} + 1} - h_{re}$	$\frac{-h_{ic}h_{oc}}{h_{fc}} + h_{rc} - 1$

		Common emitter	Common base
Common collector	h_{ic}	h_{ie}	$\frac{h_{ib}}{1 + h_{fb}}$
	h_{fc}	$-(1+h_{fe})$	$\frac{-1}{1 + h_{fb}}$
	h_{oc}	h_{oe}	$\frac{h_{ob}}{1 + h_{fb}}$
	h_{rc}	$1-h_{re} \cong 1$ (since $h_{re} << 1$)	$\frac{1-h_{ib}h_{ob}}{1 + h_{fb}}$

3.2.3 THE CONCEPT OF BIAS STABILITY

Q-point variation due to uncertainty in β :



$$I_c = \frac{\beta}{1+\beta} I_E + I_{CBO}$$

$$I_{CQ} \approx \frac{V_{BB} - V_{BE}}{R_e + \frac{R_b}{1+\beta}}$$

$$I_{CQ} \approx \frac{V_{BB} - V_{BE}}{R_e} \approx \frac{V_{BB} - 0.7}{R_e}$$

iff $R_b << \beta R_e$

The effect of temperature on the Q-point:

$$\Delta I_{CQ} = \frac{K \cdot \Delta T}{R_e} + \left(1 + \frac{R_b}{R_e}\right) I_{CBO1}(e^{K \cdot \Delta T} - 1)$$

Stability factor:

$$S_I = \frac{\Delta I_{CQ}}{\Delta I_{CBO}}, \quad S_V = \frac{\Delta I_{CQ}}{\Delta V_{BE}}, \quad S_\beta = \frac{\Delta I_{CQ}}{\Delta \beta}$$

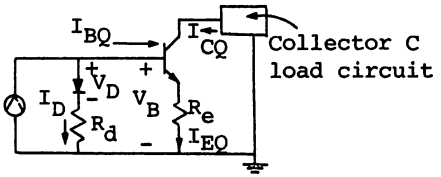
for the common-emitter amplifier:

$$S_I \tilde{=} 1 + \left(\frac{R_b}{R_e}\right), \quad S_V \tilde{=} -1/R_e, \quad \text{and} \quad S_\beta = \frac{I_{CQ_1}}{\beta_1}\left(\frac{R_b + R_e}{R_b + (1+\beta_2)Re}\right)$$

where $\beta_1, \beta_2, I_{CQ_1}$ and I_{CQ_2} are the lower and upper limits.

Temperature compensation using diode biasing:

Single diode compensations:



This compensation reduces the base-emitter voltage variation.

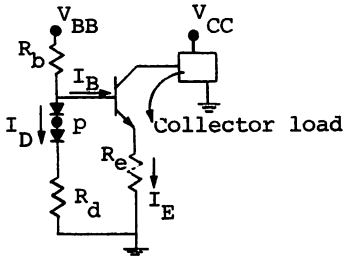
The diode is such that: $\frac{\Delta V_D}{\Delta T} = \frac{\Delta V_{BE}}{\Delta T}$.

$$I_{BB} = I_D + \frac{I_{EQ}}{1+\beta} = \text{constant}$$

$$V_B = V_D + I_D \cdot R_d = V_{BEQ} + I_{EQ} \cdot R_e$$

$$I_{EQ} = \frac{V_D - V_{BEQ} + I_D R_d}{R_e + R_d/(1+\beta)} \quad \text{and} \quad \frac{\Delta I_{EQ}}{\Delta T} = 0$$

Two-diode compensation:



The quiescent emitter current is independent of variations of temperature if $R_b = R_d$.

$$I_{EQ} = \frac{(V_{BB} \cdot R_d + 2V_D \cdot R_b)/(R_b + R_d) - V_{BEQ}}{R_e}$$

CHAPTER 4

POWER SUPPLIES

4.1 DIODE RECTIFIERS

4.1.1 HALF-WAVE RECTIFIER

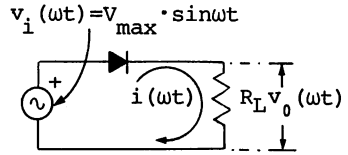


Fig. (a) Circuit

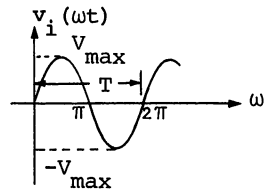


Fig. (b) Input waveform

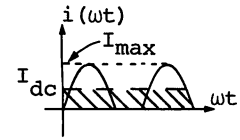


Fig. (c) Output Current

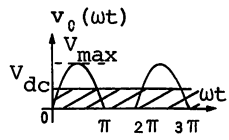


Fig. (d) Output voltage

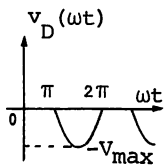


Fig. (e) Voltage across the diode

$$I_{dc} = \frac{I_{max}}{\pi} = 0.318\, I_{max}$$

$$v_{dc} = 0.318\ I_{max} \cdot R_L = 0.318\ V_{max}$$

4.1.2 FULL-WAVE RECTIFIER

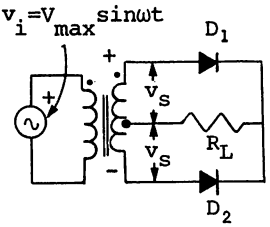


Fig. (a) Circuit

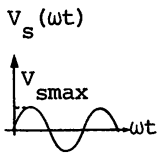


Fig. (b) Waveform across secondary winding

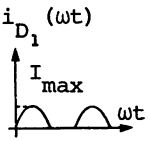


Fig. (c) Current in diode D_1

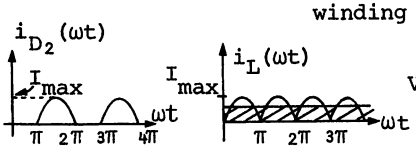


Fig. (e) Load Current

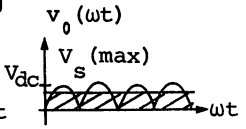


Fig. (f) Output voltage waveform

$$I_{dc} = \frac{2 \cdot I_{max}}{\pi} = 0.636\ I_{max}$$

$$V_{dc} = 0.636\ V_{max}$$

4.1.3 PIV RATING

The PIV rating indicates the voltage which a rectifier diode can withstand in a reverse bias condition.

$$PIV = 2 \cdot V_{max}$$ - for conventional full-wave rectifier

$$= V_{max}$$ - for the bridge rectifier

4.1.4 RIPPLE FACTOR

$$\text{Ripple factor (RF)} = \frac{\text{rms value of the ac component}}{\text{dc value of the waveform}}$$

$i_{ac} = i_L - i_{dc}$ (i_L = the rectified load current)

$$I_{ac(rms)} = [I^2_{L(rms)} - I^2_{dc}]^{\frac{1}{2}}$$

$$RF = \left[\left(\frac{V_{L\,rms}}{V_{dc}}\right)^2 - 1\right]^{\frac{1}{2}}$$

$$RF_{Halfwave} = 1.21 \quad \left(V_{Lrms} = \frac{V_{max}}{2} \text{ and } V_{dc} = \frac{V_{max}}{\pi}\right)$$

$$RF_{Fullwave} = 0.482 \quad \left(V_{L(max)} = \frac{V_{max}}{\sqrt{2}} = 0.707\, V_{max}\right)$$

$$RF_{Bridge\text{-}rectifier} = 0.482 \left(I_{L(max)} = \frac{I_{max}}{\sqrt{2}} = 0.707\, I_{max}\right)$$

4.1.5 RECTIFIER EFFICIENCY

$$\eta_R = \frac{P_{L(dc)}}{P_{i(dc)}}$$

For the half-wave rectifier:

$$P_{L(dc)} = I_{dc} \cdot V_{dc} = \left(\frac{I_{max}}{\pi}\right)^2 \cdot R_L$$

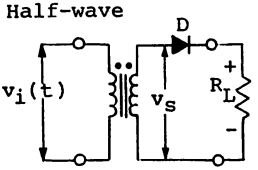
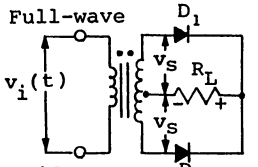
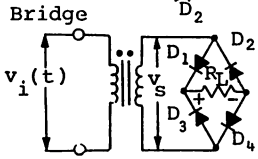
$$P_{i(ac)} = I^2_{rms} \cdot R_L = \left(\frac{I_{max}}{2}\right)^2 \cdot R_L$$

$$\eta_R = 0.406$$

For conventional and bridge rectifier:

$$\eta_R = 0.812$$

4.1.6 COMPARISON OF RECTIFIERS

Rectifier	V_{dc}	RF	f_{output}	η_R	PIV.
Half-wave 	$0.318V_{s(max)}$	1.21	f_{input}	40.6%	$V_{s(max)}$
Full-wave 	$0.636V_{s(max)}$	0.482	$2f_{input}$	81.2%	$2V_{s(max)}$
Bridge 	$0.636V_{s(max)}$	0.482	$2f_{input}$	81.2%	$V_{s(max)}$

% load regulation:

$$\%LR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

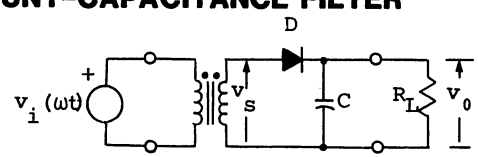
V_{NL} = No-load dc voltage

V_{FL} = Full-load dc voltage

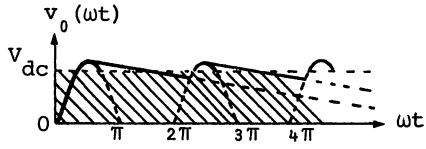
A high % LR is poor regulation.

4.2 FILTERS

4.2.1 SHUNT-CAPACITANCE FILTER

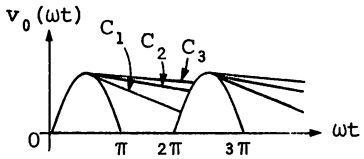


(A)



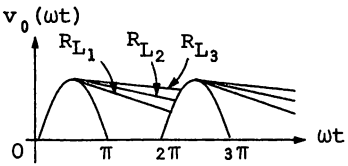
(B)

Half-wave rectifier with shunt-capacitance filter. (A) Circuit. (B) Output waveform.



$C_3 > C_2 > C_1$

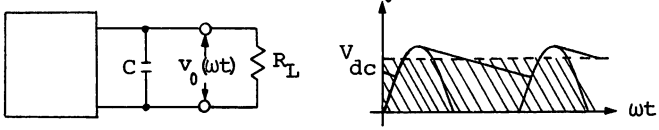
(A)



(B)

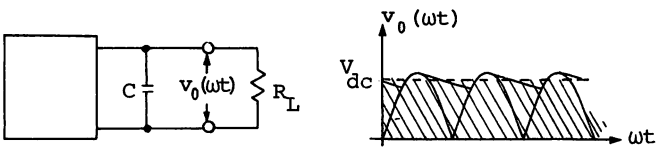
Output of Half-wave rectifier with (A) C and (B) R_L vary.

Half-Wave Rectifier



(A)

Full-Wave Rectifier



(B)

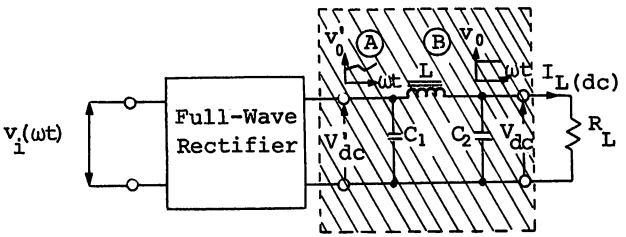
The same value of capacitance used with a full-wave rectifier in (B) produces a higher dc output than when used with a half-wave rectifier in (A).

The dc load voltage of a full-wave rectifier with a shunt-capacitance filter is given as:

$$V_{dc} = \frac{V_{s(max)}}{1 + \frac{1}{4f\ R_L\ C}}$$

$$RF = \frac{1}{4\sqrt{3} \cdot f \cdot C \cdot R_L}$$

4.2.2 Pi-FILTER

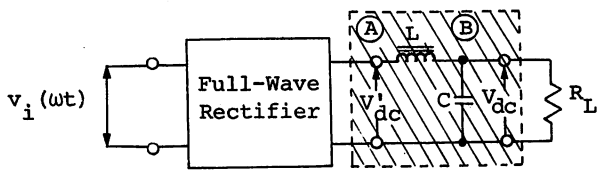


Full-wave rectifier and pi filter.

$$V_{dc} = V'_{dc} - I_{dc} \cdot r_L = \frac{V'_{dc} \cdot R_L}{R_L + r_L}$$

$$RF = \sqrt{2}/\omega^3 \cdot R_L \cdot C_1 \cdot C_2 \cdot L$$

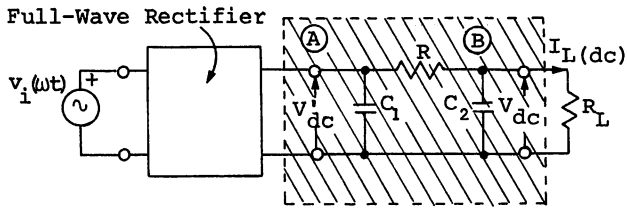
4.2.3 RC FILTER



Full-wave rectifier and L-section (choke-input) filter.

$$V_{dc} = \frac{V'_{dc} \cdot R_L}{R_L + R}$$

4.2.4 L-SECTION FILTER

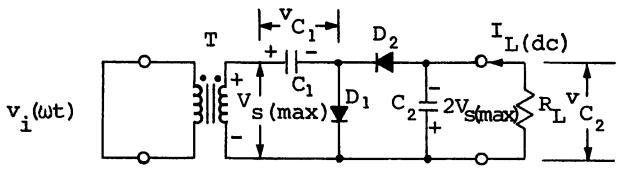


Full-wave rectifier and RC filter.

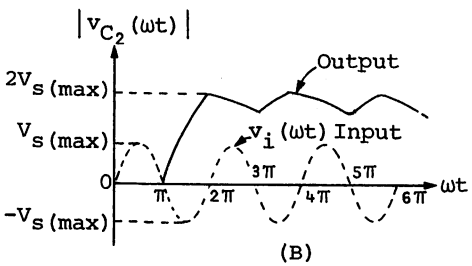
This filter is used with high-load current circuits.

4.2.5 VOLTAGE MULTIPLIER

The voltage multiplier is used when a high dc voltage with extremely light loading is required.



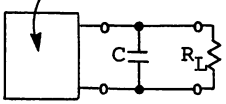
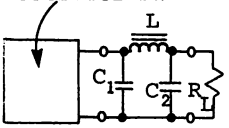
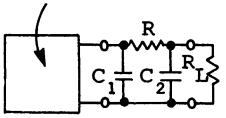
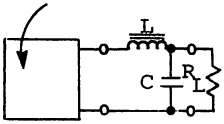
(A)



(B)

$$V_{c2} = 2V_{s(max)}$$

4.2.6 COMPARISON OF FILTERS

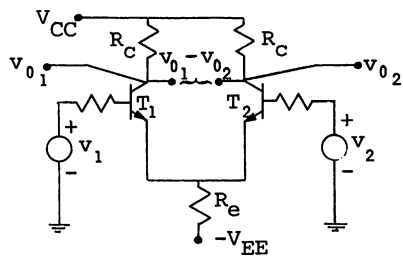
Filter	V_{dc}	RF
Shunt-Capacitance Rectifier FW  	$\frac{V_{s(max}}{1 + 1/(4fR_LC)}$ For 60 Hz: $\frac{V_{s(max)}}{0.00417/R_LC}$	$\frac{1}{4\sqrt{3}fR_LC}$ For 60 Hz: $\frac{2.41 \times 10^{-3}}{R_LC}$
Pi Rectifier FW  	$\frac{V_{s(max)}R_L/(R_L+r_L)}{1 + 1/(4fR_LC_1)}$ For 60 Hz: $\frac{V_{s(max)}R_L/(R_L+r_L)}{1 + 0.00417/R_LC}$	$\frac{\sqrt{2}}{\omega^3C_1C_2LR_L}$ For 60 Hz: $\frac{0.026}{C_1C_2R_LL} \times 10^{-6}$
RC Rectifier FW  	$\frac{V_{s(max)}R_L/(R_L+R)}{1 + 1/(4fR_LC_1)}$ For 60 Hz: $\frac{V_{s(max)}R_L/(R_L+R)}{1 + 0.00417/R_LC}$	$\frac{\sqrt{2}}{\omega^2C_1C_2R_LR}$ For 60 Hz: $\frac{9.95}{C_1C_2R_LR} \times 10^{-6}$
L-Section Rectifier FW  	$0.636V_{s(max)}$ For 60 Hz: $0.636V_s(max)$	$\frac{0.118}{(\omega^2LC)}$ For 60 Hz: $\frac{0.83}{LC} \times 10^{-6}$

CHAPTER 5

MULTITRANSISTOR CIRCUITS

5.1 THE DIFFERENCE AMPLIFIER

5.1.1 BASIC DIFFERENCE AMPLIFIER

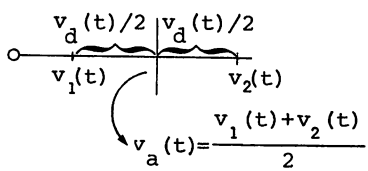


The Differential-mode or difference-mode input voltage $v_d = v_2 - v_1$.

The common-mode input voltage $V_a = \frac{V_2+V_1}{2}$.

$v_2 = v_a + \frac{v_d}{2}$

$v_1 = v_a - \frac{v_d}{2}$

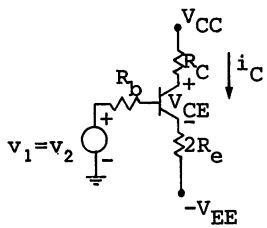


V_d is the desired signal and is amplified while V_a is rejected.

5.1.2 Q-POINT ANALYSIS

The differential-mode input is assumed to be zero. ($V_1 = V_2$)

The equivalent circuit for T_1 or T_2 when $v_1 = v_2 = v_a$:



$$v_{E_1} = v_{E_2} = (i_{E_1} + i_{E_2})R_e - V_{EE}$$

$$= i_E(2R_e) - V_{EE} \quad (\text{when } i_{E_1} = i_{E_2} = i_E)$$

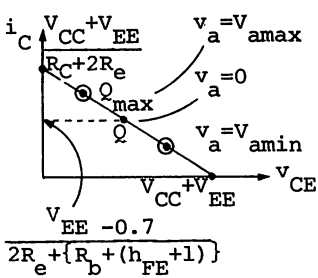
The load-line equation for $v_a = v_1 = v_2$ is

$$v_{CE} = V_{CC} - i_C R_C - i_E(2R_e) + V_{EE}$$

$$\approx V_{CC} + V_{EE} - i_C(R_C + 2R_e)$$

$$i_C \approx \frac{v_a + V_{EE} - 0.7}{2R_e + [R_b \div (h_{FE}+1)]}, \quad (V_{BE} = 0.7))$$

5.1.3 COMMON-MODE LOAD LINE



The common-mode input $v_a = 0$, for Q.

$Q = Q_{max}$ when $v_a = v_{amax}$;

$Q = Q_{min}$ when $v_a = v_{amin}$.

In both cases, $v_d = 0$.

The individual collector voltages v_{01} and v_{02} will vary with variations in v_a.

Difference-mode load-line equations

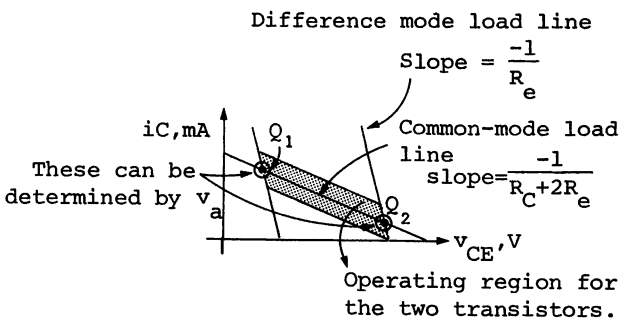
These equations determine the effect of a non-zero difference-mode input. ($v_2 = -v_1 = \frac{v_d}{2}$, $v_a = 0$ and Q is as shown in the previous figure.)

$\Delta v_{CE_1} = -R_c \cdot \Delta i_{c_1}$, using small-signal notation

$$\boxed{v_{ce_1} = -R_c \cdot i_{c_1}}, \quad \Delta v_{CE_2} = -R_c \cdot \Delta i_{c_2},$$

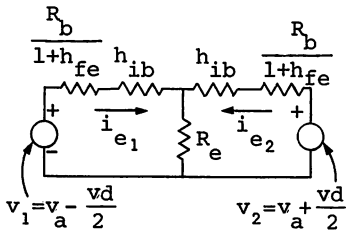
or $$\boxed{v_{ce_2} = -R_c \cdot i_{c_2}}$$

These are "Difference-mode load line" equations, such that $v_{E_1} = v_{E_2}$.

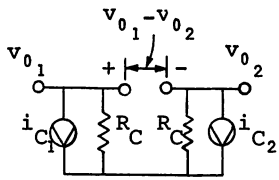


Small-signal analysis:

Equivalent circuit with all components reflected into emmiter.

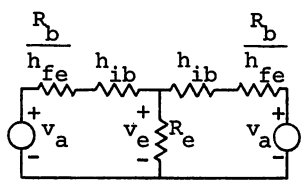


(a) Input circuit

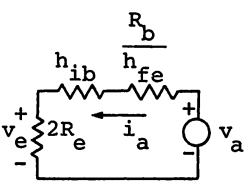


(b) Output circuit

Circuit used to calculate i_a and i_d:

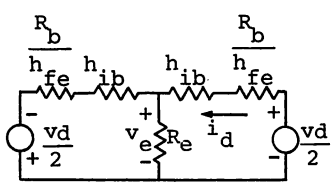


(a) To calculate i_a

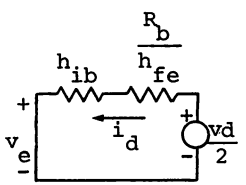


(b) Reduced equi, circuit

$$i_a = v_a / 2R_e + h_{ib} + [R_b \div (h_{fe} + 1)]$$



(a) To calculate i_d



(b) Reduced equivalent circuit

$$i_d = \frac{v_d/2}{h_{ib} + [R_b \div (1+h_{fe})]}$$

Assuming $i_c \approx i_e$, and $v_{01} - v_{02} = \frac{R_c}{h_{ib} + [R_b \div (1+h_{fe})]} \cdot v_d$

Common-mode Rejection Ratio:

$$A_d = \text{The difference-mode gain} = \frac{R_c/2}{h_{ib}+[R_b \div (1+h_{fe})]}$$

$$A_a = \text{The common-mode gain} = \frac{R_c}{2R_e+h_{ib}+[R_b \div (1+h_{fe})]}$$

$$v_{01} = A_d \cdot V_d - A_a \cdot V_a \text{ and } v_{02} = -A_d \cdot v_d - A_a \cdot v_a.$$

Common-mode rejection ratio:

$$\text{"CMRR"} = \frac{A_d}{A_a} \cong \frac{R_e}{h_{ib}+[R_b/h_{fe})}$$

If "CMRR" >> $\frac{V_a}{V_d}$, then the output voltage is proportional to V_d.

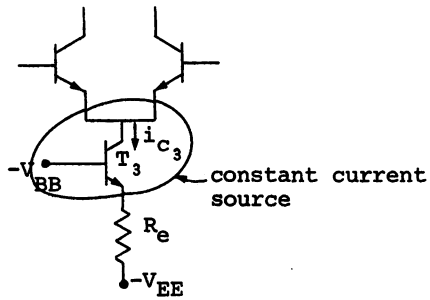
5.1.4 DIFFERENCE AMPLIFIER WITH CONSTANT CURRENT SOURCE

$$CMRR = \frac{R_e}{(V_T/I_{EQ})+(R_b/h_{fe})}, \text{ if } \frac{R_b}{h_{fe}} \text{ is small,}$$

$$CMRR < \frac{R_e \cdot I_{EQ}}{V_T}$$

CMRR can be increased only by increasing R_e.

In the previous circuit, R_e is replaced by another transistor which is a constant-current source.



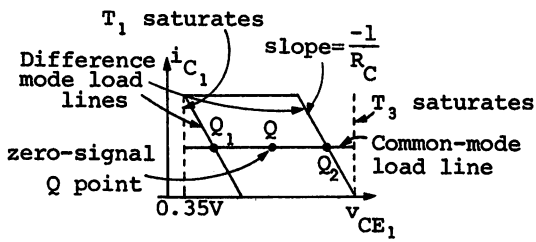
Quiescent operation:

$$I_{CQ_3} \approx \frac{V_{EE} - V_{BB} - 0.7}{R_e} \quad (I_{CQ_3} \text{ is constant as long as } T_3 \text{ does not saturate.})$$

The condition for keeping T_3 in the linear region is:

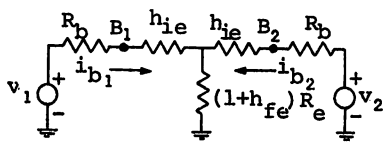
$$v_{CE} > V_T \left[2 \cdot 2 + \ln \left(\frac{h_{fe}}{h_{fe}} \right) \right]$$

Load-lines that describe circuit operation:



$(V_{CEQ_3} \geq 0.35V)$

Small-signal operation:

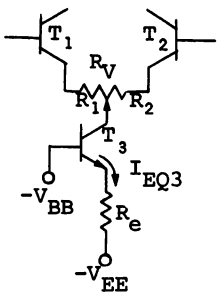


Equivalent circuit looking into the bases

The input impedance R_i between the bases of T_1 and T_2 is:

$$R_i = 2 \cdot h_{ie}.$$

5.1.5 DIFFERENCE AMPLIFIER WITH EMITTER RESISTORS FOR BALANCE



Difference amplifier with balance control R_U.

To compensate for different h_{fe1} and h_{fe2}, R_v is used when T_1 and T_2 have different characteristics.

The condition which ensures that the emitter currents of T_1 and T_2 are the same is:

$$R_2 - R_1 = R_b\left(\frac{1}{h_{fe1}} - \frac{1}{h_{fe2}}\right).$$

R_v results in symmetrical operation but it causes a loss in the current gain.

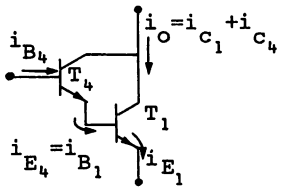
$$A_d = \frac{R_c}{R_b\left(\frac{1}{h_{fe1}} + \frac{1}{h_{fe2}}\right) + 2h_{ib} + Rv},$$

if

$$(R_e)_{eff} \approx \frac{1}{h_{ob_3}} >> h_{ib_1} + \frac{R_b}{h_{fe_1}} + R_1$$

5.2 THE DARLINGTON AMPLIFIER

The Darlington amplifier is used to provide increased input impedance and a very high current gain ($h_{fe_1}.h_{fe_2}$).



Basic Darlington amplifier

Current gain $A_i = \alpha(1+h_{fe})^2 + \alpha(1+h_{fe}) = \alpha(1+h_{fe})(h_{fe}+2)$

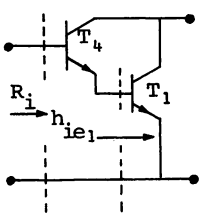
$\approx h_{fe}^2$ (assuming identical transistors)

$$R_i = h_{ie_4} + (1+h_{fe})h_{ie_1}$$

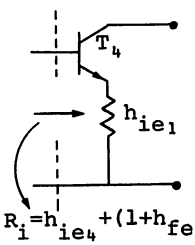
$$= \frac{(1+h_{fe})V_T}{I_{EQ_4}} + \frac{(1+h_{fe})^2 \cdot V_T}{I_{EQ_1}}$$

$$= 2(1 + h_{fe})h_{ie_1} = 2 \cdot h_{ie_4}$$

Input impedance:



(a) Darlington amplifier



(b) T_1 replaced by h_{ie_1}

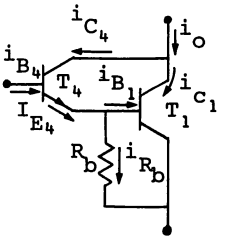
In this case, emitter current in T_4 can be adjusted by setting

$$R_b, I_{EQ_4} = I_{BQ_1} + \frac{0.7}{R_b}$$

$$R_i = h_{ie_4} + (1+h_{fe})(R_b \,||\, h_{ie_1})$$

$$i_0 = h_{fe} \cdot i_{b_4} + h_{fe}(1 + h_{fe})i_{b_4} \cdot \frac{R_b}{R_b + h_{ie_1}}$$

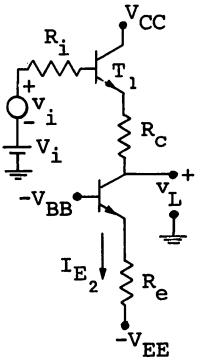
$$A_i = h_{fe}^2 \frac{R_b}{R_b + h_{ie}} + h_{fe} \cdot \left(1 + \frac{R_b}{R_b + h_{ie_1}}\right)$$



Darlington amplifier with bias resistor.

5.3 THE CASCADE AMPLIFIER

The Amplifier:



The cascade amplifier is used as a dc level shifter when

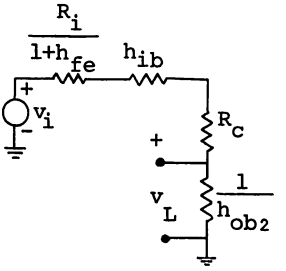
the voltage of interest consists of a small-signal ac component v_i and a fixed dc level V_i. v_i from the level shifter should have a dc level different from V_i. Typically this final output level is to be OV.

DC analysis:

T_1 is the emitter follower and T_2 acts as a constant current source. DC component of the output voltage, V_L:

$$V_i - \frac{R_i I_{E2}}{1+h_{fe}} - 0.7 - R_c \cdot I_{E2}$$

Small-signal analysis:

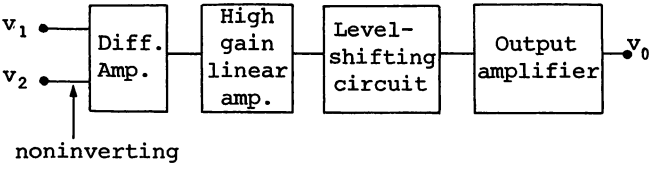


$$v_L \text{ (small-signal component of the output voltage)} \cong \frac{v_i}{1 + \frac{(R_i \div h_{fe}) + h_{ib} + R_c}{1 \,/\, h_{ob2}}}$$

Since $\frac{1}{h_{ob2}}$ is much larger than $\frac{R_i}{h_{fe}} + h_{ib} + R_c$, the load voltage $v_L \approx v_i$, while a negligible attenuation of the signal has resulted from the shift in dc level.

5.4 THE OP AMPLIFIER

Typical configuration:

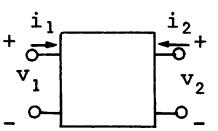


CHAPTER 6

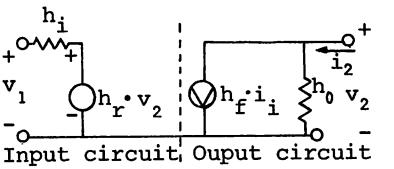
SMALL-SIGNAL, LOW-FREQUENCY ANALYSIS AND DESIGN

6.1 HYBRID PARAMETERS

6.1.1 GENERAL TWO-PORT NETWORK



(a) Two-part network



(b) Equivalent circuit of two-part network.

6.1.2 HYBRID EQUATIONS

$$v_1 = h_i \cdot i_1 + h_r \cdot v_2 \qquad v_1 = h_{11} \cdot i_1 + h_{12} \cdot v_2$$

$$i_2 = h_f \cdot i_1 + h_0 \cdot v_2 \qquad i_2 = h_{21} \cdot i_1 + h_{22} \cdot v_2$$

6.1.3 TERMINAL DEFINITIONS FOR H-PARAMETERS

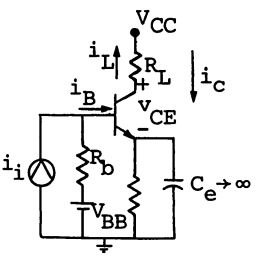
$$h_i = \left.\frac{v_1}{i_1}\right|_{v_2 = 0}$$ = short-circuit input impedance

$$h_r = \left.\frac{v_1}{v_2}\right|_{i_1 = 0}$$ = open-circuit reverse voltage gain

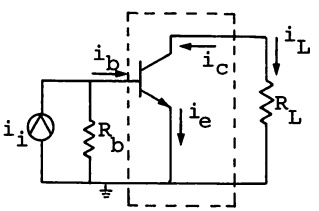
$$h_f = \left.\frac{i_2}{i_1}\right|_{v_2 = 0}$$ = short-circuit forward current gain

$$h_0 = \left.\frac{i_2}{v_2}\right|_{i_1 = 0}$$ = open-circuit output admittance

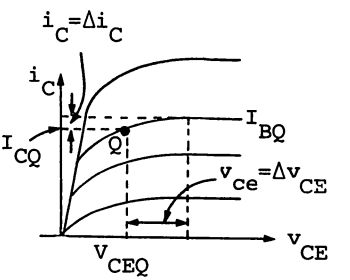
6.2 THE C-E CONFIGURATION



(a) Complete circuit



(b) Small-signal circuit



(c) v_i characteristics

$$h_{oe} = \left.\frac{i_c}{v_{ce}}\right|_{ib=0} = \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{Q\ point}$$

where i_c and v_{ce} are small variations about nominal operating point.

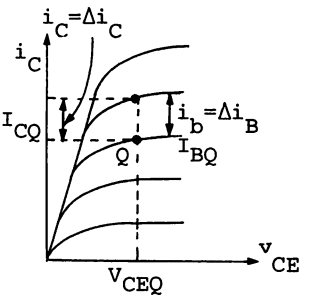
$$h_{oe} = \frac{h_{FE}}{h_{FC}} \cdot \frac{I_{CQ}}{V_T}\left[\frac{e^{v_{CE}/V_T}}{[e^{v_{CE}/V_T} + h_{FE}/h_{FC}]^2}\right]$$

$$\simeq \frac{h_{FE}}{h_{FC}} \quad \frac{I_{CQ}}{V_T}\, e^{-v_{CE}/V_T}$$

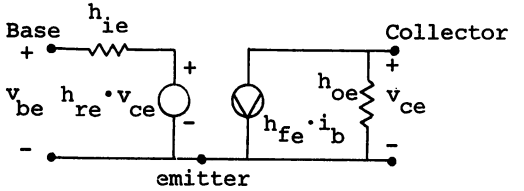
$$h_{fe} = \left.\frac{i_c}{i_b}\right|_{Q\ point} = \left.\frac{\Delta i_C}{\Delta i_B}\right|_{Q\ point}$$

$$h_{ie} = \left.\frac{v_{be}}{i_b}\right|_{v_{CE}=0} = \left.\frac{v_{be}}{i_b}\right|_{Q\ point}$$

$$= \frac{V_T}{I_{BQ}} \simeq h_{fe} \cdot \frac{V_T}{I_{CQ}} \simeq h_{fe} \cdot \frac{V_T}{I_{EQ}}$$

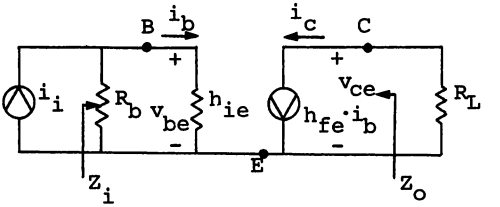


Equivalent circuit:



This diagram can be simplified by ignoring h_{oe} and h_{re}.

C-E amplifier equivalent circuit:



$$\frac{i_b}{i_i} = \frac{R_b}{R_b + h_{ie}}$$

$$A_i = \frac{i_L}{i_i} = \frac{-h_{fe}}{1 + h_{fe}[(25 \times 10^{-3})/I_{EQ} R_b]}$$

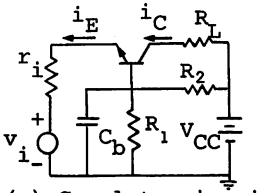
Requirement of high gain and stability:

$$h_{ie} = h_{fe} \cdot \frac{V_T}{I_{EQ}} << R_b << h_{fe} \cdot R_e$$

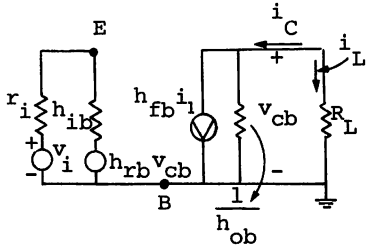
$$Z_i = \frac{R_b h_{ie}}{R_b + h_{ie}} \approx h_{ie} \quad (\text{if } R_b >> h_{ie})$$

$$Z_0 = \left. \frac{v_{ce}}{i_c} \right|_{i_i = 0} = 1/h_{oe}$$

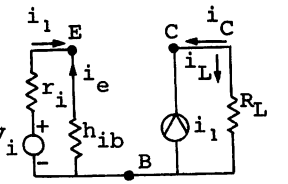
6.3 THE C-B CONFIGURATION



(a) Complete circuit



(b) Hybrid model



(c) Simplified circuit

For the hybrid model:

$$V_{eb} = h_{ib}i_1 + h_{rb} \cdot v_{cb} = h_{ib}(-i_e) + h_{rb} \cdot v_{cb}$$

$$i_c = h_{fb} \cdot i_1 + h_{ob} \cdot v_{cb} = h_{fb}(-i_e) + h_{ob} \cdot v_{cb}$$

$$h_{ib} = \frac{v_{eb}}{-i_e}\bigg|_{v_{cb}=0} = \frac{V_T}{I_{EQ}} \approx \frac{h_{ie}}{1+h_{fe}}$$

$$h_{fb} = \frac{i_c}{i_1}\bigg|_{v_{cb}=0} = \frac{i_c}{-i_e}\bigg|_{v_{cb}=0} = -\alpha$$

$$h_{ob} = \frac{i_c}{v_{cb}}\bigg|_{i_e=i_1=0}$$

Simplified equivalent circuit:

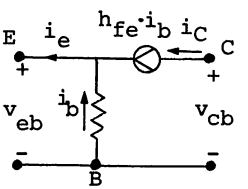
$$i_e = (1 + h_{fe})i_b = (i + h_{fe})\left(\frac{-v_{eb}}{h_{ie}}\right)$$

$$h_{ib} = \left.\frac{-v_{eb}}{i_e}\right|_{v_{cb}=0} = \frac{h_{ie}}{1+h_{fe}} \approx \frac{h_{ie}}{h_{fe}}$$

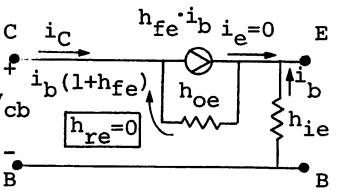
$$h_{fb} \text{ (short-circuit current gain)} = \left.\frac{i_c}{-i_e}\right|_{v_{cb}=0} = \frac{-h_{fe}}{1+h_{fe}} \doteq -1$$

$$h_{ob} \approx \frac{h_{oe}}{h_{fe}}$$

Modified circuits:



CE ckt. for finding 'h' parameters of C-B configuration.



C-B equivalent for finding h_{ob}.

To find the CB parameters h_{ob}, h_{fb}, and h_{ib}, divide the corresponding CE parameters by $1 + h_{fe}$.

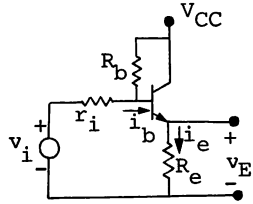
6.4 THE C-C (EMITTER-FOLLOWER) CONFIGURATION

Characteristics:

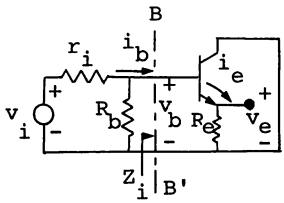
A) A voltage gain slightly less than unity;

B) A high input impedance, and

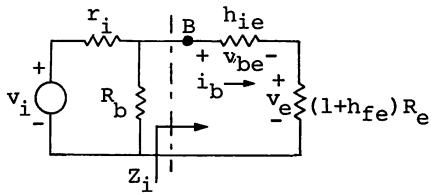
C) A low output impedance.



(a) Emitter-follower.



(b) A.C. circuit

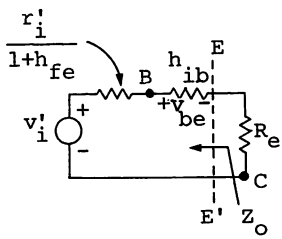


(c) Equivalent circuit

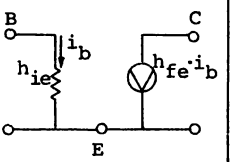
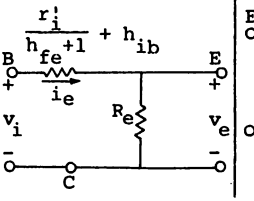
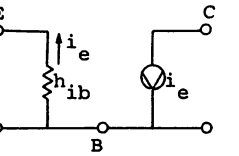
$$A_v = \frac{v_e}{v_i} = \frac{R_b}{r_i+R_b}\left[\frac{1}{1+[h_{ie}+(r_i \| R_b)]/[(1+h_{fe})R_e]}\right]$$

$$Z_i = h_{ie} + (1 + h_{fe})R_e$$

$$Z_0 = h_{ib} + \frac{r_i}{1+h_{fe}}$$

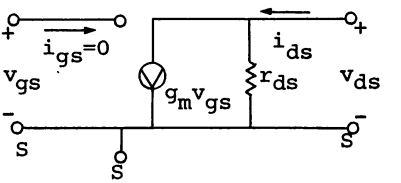


6.5 SIGNIFICANT PARAMETERS

	Configuration		
	CE	EF(CC)	CB
Gain	$A_i \approx -h_{fe}$	$A_v \approx 1$	$A_i \approx -h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$
Input impedance	$h_{ie} = \frac{(25\times10^{-3})h_{fe}}{I_{EQ}}$	$Z_i = h_{ie} + (h_{fe}+1)R_e$	$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$
Output impedance	$\frac{1}{h_{oe}} > 10^4\Omega$	$Z_o \approx h_{ib} + \frac{r_i'}{h_{fe}+1}$	$\frac{1}{h_{ob}} = \frac{1+h_{fe}}{h_{oe}}$
Simplest equivalent circuit			

6.6 SMALL-SIGNAL EQUIVALENT CIRCUIT OF THE FET

6.6.1 EQUIVALENT CIRCUIT



6.6.2 TRANSCONDUCTANCE

$$g_m = \left.\frac{\partial i_{DS}}{\partial v_{GS}}\right|_{Q\ \text{point}}$$

For the MOSFET:

$$i_{DS} = k_n(V_{GS}-V_T)^2, \text{ and } g_m = 2k_n(V_{GS}-V_T)\Big|_{V_{GSQ}}$$

$$= 2\sqrt{k_n \cdot I_{DSQ}}$$

g_m of a FET is analogous to $1/h_{ib}$ in BJT:

$$\left(\frac{1}{h_{ib}}\right)_{BJT} >> (g_m)_{FET}$$

6.6.3 DRAIN SOURCE RESISTANCE

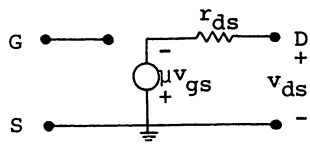
$$r_{ds} = \frac{\partial V_{DS}}{\partial i_{DS}}\Bigg|_{Q \text{ point}} \quad \alpha \frac{1}{I_{DQ}}$$

The drain source resistance is analogous to h_{oe} of the transistor.

6.6.4 AMPLIFICATION FACTOR

$$\mu = \frac{-\partial v_{DS}}{\partial v_{GS}}\Bigg|_{Q \text{ point}} = g_m \cdot r_{ds}$$

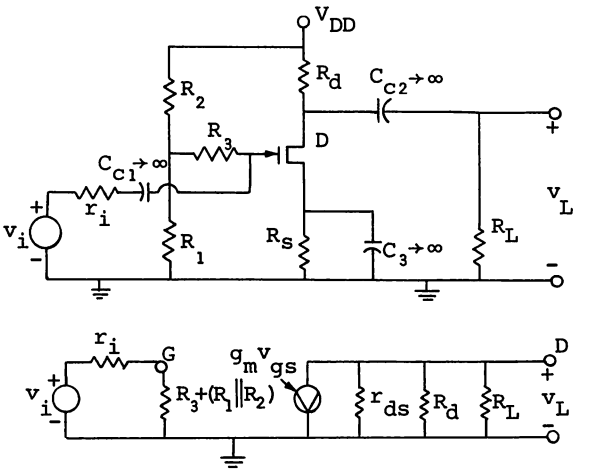
Equivalent Model:



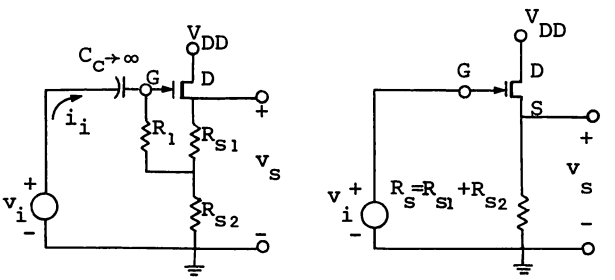
6.7 THE COMMON-SOURCE VOLTAGE AMPLIFIER

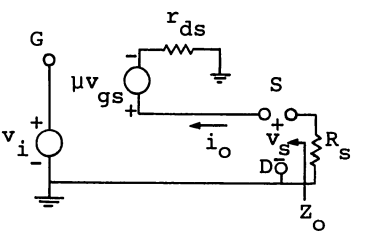
$$A_v = \frac{V_L}{V_i} = -g_m(R_L || Z_0)\left(\frac{1}{1+[r_i \div (R_3+(R_1||R_2)]}\right)$$

with $r_i \ll R_3 + (R_1 \| R_2)$ and $R_L \ll Z_0$, $A_V \doteq -g_m R_L$



6.8 THE COMMON-DRAIN VOLTAGE AMPLIFIER (THE SOURCE FOLLOWER)





Equivalent circuit

$$Z_0 = \left.\frac{v_s}{i}\right|_{v_i=0} \quad \text{(as seen by } R_s\text{)} = \frac{r_{ds}}{1+\mu} \approx 1/g_m$$

(when $\mu = g_m \cdot r_{ds} >> 1$)

$$A'_v \text{ (open-circuit voltage gain)} = \frac{\mu}{1+\mu} \cong 1, \text{ when } \mu >> 1$$

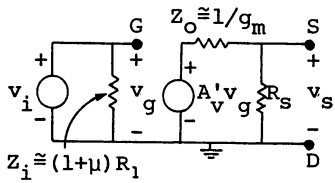
$$A_v = \frac{v_s}{v_i} = \frac{\mu}{1+\mu}\left[\frac{g_m \cdot R_s}{1+g_m \cdot R_s}\right]$$

$$Z_i = \frac{v_g}{i_i} \cong \frac{R_1}{1 - \left(\frac{v_s}{v_g}\right)\left[\frac{R_{s_2}}{R_{s_1}+R_{s_2}}\right]}$$

$$Z_{02} \text{ (looking into the source)} \cong \frac{R_s(r_{ds}+R_s)}{r_{ds}+(2+\mu)R_s}$$

$$\cong \frac{r_{ds}+R_s}{\mu}$$

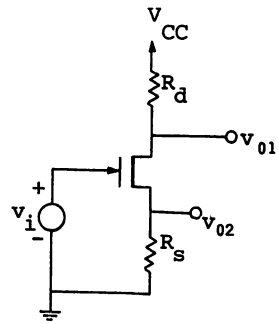
Equivalent circuit for Z_i:



Assuming $R_{s_2} >> R_{s_1}$,

$$Z_i \cong (1+\mu)R_1$$

6.9 THE PHASE-SPLITTING CIRCUIT



$$v_{01} = \frac{-\mu \cdot R_d}{(1+\mu)R_s + r_{ds} + R_d} \, v_i$$

$$v_{02} = \frac{(\mu/1+\mu)R_S}{R_s + \left(\frac{r_{ds}}{1+\mu}\right) + \frac{R_d}{1+\mu}} \, v_i$$

Z_{01} (looking into the source) $\cong \dfrac{R_s[r_{ds}+(1+\mu)R_s]}{r_{ds}+(2+\mu)R_s}$

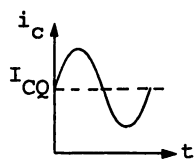
$\cong R_s$

CHAPTER 7

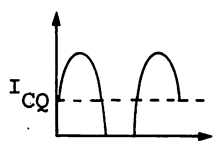
AUDIO-FREQUENCY LINEAR POWER AMPLIFIERS

7.1 THE CLASS A COMMON-EMITTER POWER AMPLIFIER

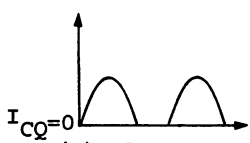
The power amplifiers are classified according to the portion of the input sine wave cycle during which the load current flows.



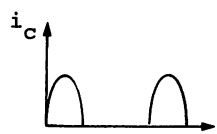
(a) Class A



(b) Class AB

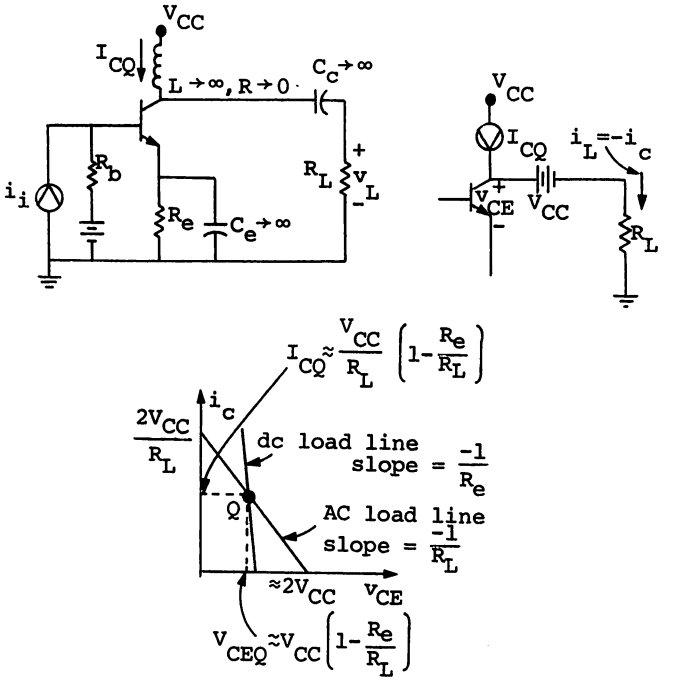


(c) Class B



(d) Class C current flows for less than one-half cycle

Q-point placement:



DC-load-line equation:

$$V_{CC} = v_{CE} + i_C \cdot R_e$$

AC-load-line equation:

$$v_{ce} = -i_c R_L = i_L \cdot R_L$$

or

$$i_C - I_{CQ} = \frac{-1}{R_L}(v_{CE} - V_{CEQ})$$

To place "Q" for the maximum symmetrical swing

$$I_{CQ} = \frac{V_{CC}}{R_{ac}+R_{dc}}$$

$$\approx V_{CC}/R_L$$

$$V_{CEQ} = V_{CC} \frac{R_L}{R_L + R_e} = \frac{V_{CC}}{1+(R_e/R_L)}$$

$$\approx V_{CC} \text{ (because } R_L >> R_e)$$

Power calculations:

$$i_C = I_{CQ} + i_c = \frac{V_{CC}}{R_L} + i_c$$

$$i_L = -i_c$$

$$i_{supply} = i_L + i_C = I_{CQ} = \frac{V_{CC}}{R_L}$$

$$v_{CE} = V_{CC} - i_C R_L, \quad v_L = i_L R_L = -i_C R_L$$

For a sinusoidal signal current:

$$i_i = I_{im} \cdot \sin \omega t, \quad i_c = I_{cm} \cdot \sin \omega t$$

Supplied power $P_{CC} = V_{CC} \cdot I_{CQ} \approx \frac{V_{CC}^2}{R_L}$

Power transferred to load:

$$P_L = \frac{I_{LM}^2 \cdot R_L}{2} = \frac{I_{cm}^2 \cdot R_L}{2}$$

(since $i_L = -i_C$, $I_{LM} = -I_{cm}$).

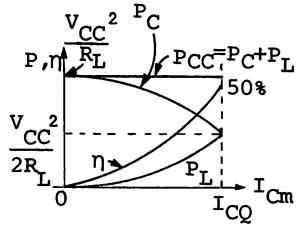
$$P_{Lmax} = \frac{I_{CQ}^2 \cdot R_L}{2} = \frac{V_{CC}^2}{2R_L} \quad \text{(when } I_{cm} = I_{CQ}\text{)}.$$

Collector dissipation:

$$P_C = P_{CC} - P_L = \frac{V_{CC}^2}{R_L} - \frac{I_{cm}^2 \cdot R_L}{2}$$

$$P_{Cmin} = V_{CC}^2/2R_L \text{ and } P_{Cmax} = \frac{V_{CC}^2}{R_L} = V_{CEQ} I_{CQ}$$

Efficiency:



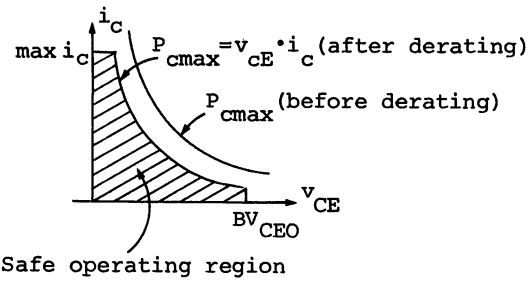
Variation of power and efficiency with collector current

$$\eta = \frac{P_L}{P_{CC}} = \frac{I_{cm}^2(R_L/2)}{V_{CC} \cdot I_{CQ}} = \frac{1}{2}\left(\frac{I_{cm}}{I_{CQ}}\right)^2$$

$\eta_{max} = 50\%$

Figure of merit $= \frac{P_{Cmax}}{P_{L\,max}} = 2.$

The maximum-dissipation hyperbola:



For the safe operation, the Q-point must lie on or below the hyperbola $v_{CE} \cdot i_c = P_{c_1max}$.

This hyperbola represents the locus of all operating points at which the collector dissipation is exactly P_{cmax}.

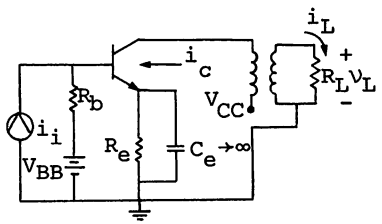
The ac load line, with slope $\frac{-1}{R_L}$, must pass through the Q-point, intersect the v_{CE} at a voltage less than BV_{CEO} and intersect the i_c axis at a current less than max i_c, i.e.,

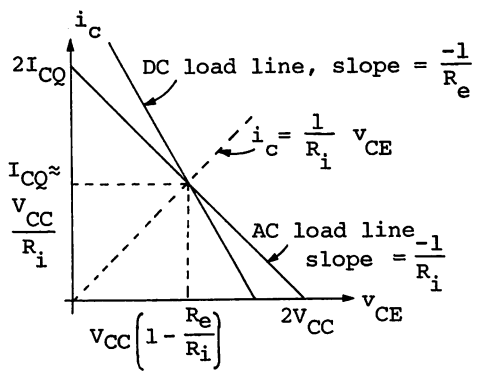
$$2\,V_{CC} \leq BV_{CEO},$$

$$2\,I_{CQ} \leq i_{cmax}.$$

$$\text{Slope of hyperbola}\Big|_{\text{Q point}} = \frac{\partial i_c}{\partial v_{CE}} = \frac{-I_{CQ}}{V_{CEQ}} = \frac{-1}{R_L}$$

7.2 THE TRANSFORMER-COUPLED AMPLIFIER





Load lines:

DC Load line: $V_{CC} = v_{CE} + i_E \cdot R_e \approx v_{CE} + i_c R_e$

AC load line: $\text{Slope} = \frac{i_c}{v_{ce}} = \frac{-1}{R'_L}$ (where $R'_L = N^2 R_L$).

$$I_{CQ} \approx \frac{V_{CC}}{R'_L}\left(1 - \frac{R_e}{R'_L}\right), \quad V_{CEQ} \approx V_{CC}\left(1 - \frac{R_e}{R'_L}\right)$$

Power calculations:

The signal i_L is sinusoidal; thus,

$$i_c = I_{cm} \cdot \sin \omega t.$$

Supplied power: $P_{CC} = V_{CC} \cdot I_{CQ} = \frac{V_{CC}^2}{R'_L}$

Load power:

$$P_L = \frac{I_{LM}^2}{2} \qquad R_L = \frac{I_{cm}^2}{2} R'_L, \quad (I_{LM} = N \cdot I_{CM})$$

$$P_{Lmax} = \frac{V_{CC}^2}{2R'_L}$$

Collector dissipation:

$$P_C = \frac{V_{CC}^2}{R'_L} - \frac{I_{cm}^2}{2} R'_L$$

$$P_{cmax} = \frac{V_{CC}^2}{R'_L} = V_{CEQ} \cdot I_{CQ}$$

Efficiency:

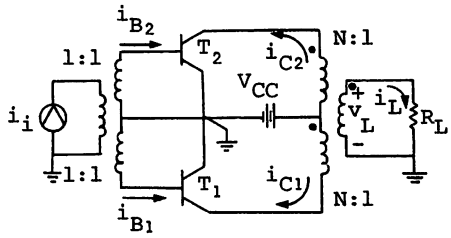
$$\eta = \frac{1}{2}\left(\frac{I_{cm}}{I_{CQ}}\right)^2$$

$$\eta_{max} = 50\%$$

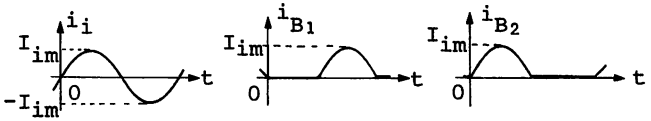
$$\text{Fig. of merit} = \frac{P_{cmax}}{P_{Lmax}} = 2.$$

7.3 CLASS B PUSH-PULL POWER AMPLIFIERS

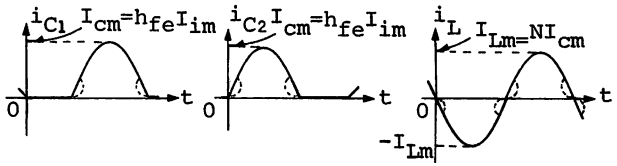
Circuit:



Waveforms:

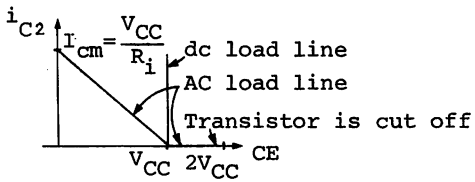


(a) Input current (b) Base current in T_1 (c) in T_2



(d) Collector current in T_1 (e) Collector current in T_2 (f) Load current

Load-line determination:



DC load line: $v_{CE} = V_{CC}$

AC load line: $$\text{Slope} = \frac{i_c}{CE} = \frac{-1}{R'_L}$$

The maximum value of both i_{c_1} and i_{c_2} is $I_{cm} = \frac{V_{CC}}{R'_L}$.

Power calculations:

$$i_i = I_{im} \cdot \sin \omega t$$

$$\text{Supplied power} = P_{CC} = \frac{2}{\pi} \cdot V_{CC} \cdot I_{cm}$$

$$P_{CC(max)} = \frac{2}{\pi} V_{CC} \cdot \frac{V_{CC}}{R'_L} = \frac{2 V_{CC}^2}{\pi \cdot R'_L}$$

$$P_L = \frac{1}{2} I_{cm}^2 \cdot R'_L, \qquad P_{L,\max} = \frac{V_{CC}^2}{2R'_L}$$

Power dissipated in the collector:

$$2P_C = \frac{2}{\pi} V_{CC} \cdot I_{cm} - \frac{R'_L \cdot I_{cm}^2}{2} = P_{CC} - P_L$$

$$I_{cm} = \frac{2}{\pi} \cdot \frac{V_{CC}}{R'_L}$$ (The collector current at which the collector dissipation is maximum)

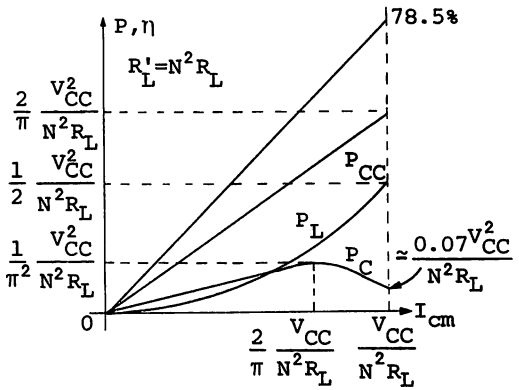
$$2P_{cmax} = \frac{2}{\pi^2} \cdot \frac{V_{CC}^2}{R'_L}$$

Efficiency: $$\eta = \frac{P_L}{P_{CC}} = \frac{\pi}{4} \quad \frac{I_{cm}}{V_{CC}/R'_L}$$

$$\boxed{\eta_{max} = \frac{\pi}{4} = 78.5\%}$$

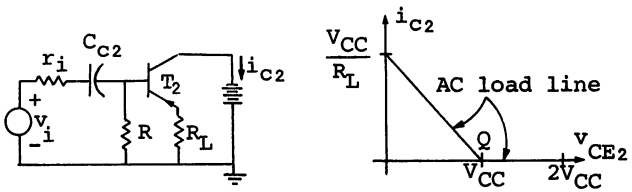
Figure of merit: $$\frac{P_{cmax}}{P_{Lmax}} = \frac{2}{\pi^2} \approx \frac{1}{5}$$

Power and efficiency variation:

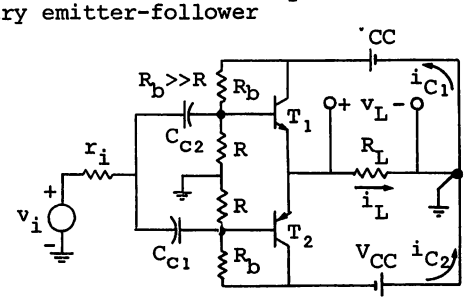


7.4 AMPLIFIERS USING COMPLEMENTARY SYMMETRY

The circuit:



Circuit and load line for T_2 of complementary-symmetry emitter-follower



Complementary-symmetry amplifier

Each transistor is essentially a class "B" emitter follower.

$$i_L = i_{C_1} - i_{C_2}$$

$$I_{cm} = \frac{V_{CC}}{R_L}$$ (If v_i is sinusoidal, i_L is also sinusoidal.)

$$i_L = I_{CM} \cdot \sin \omega t$$

$$= \frac{V_{CC}}{R_L} \cdot \sin \omega t.$$

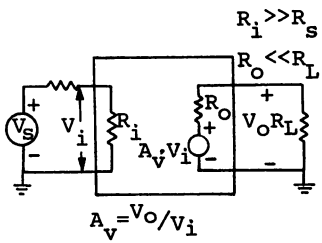
$$P_{L,max} = \frac{V_{CC}^2}{2R_L}$$

CHAPTER 8

FEEDBACK AMPLIFIERS

8.1 CLASSIFICATION OF AMPLIFIERS

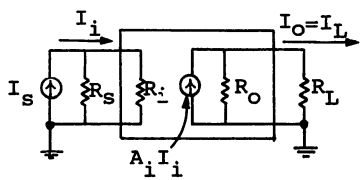
8.1.1 VOLTAGE AMPLIFIER



The voltage amplifier provides a voltage output proportional to the voltage input. The proportionality factor is independent of the source and load impedances. For the ideal amplifier:

$$R_i = \infty, \quad R_o = 0, \quad A_v = \frac{V_0}{v_s}$$

8.1.2 CURRENT AMPLIFIER

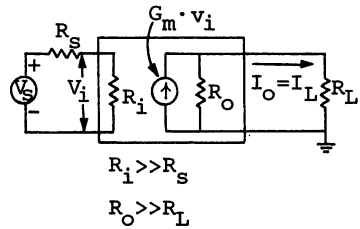


Norton's equivalent circuit of a current amplifier.

$$A_i = \frac{I_L}{I_i}$$ (with $R_i = 0$ representing the short-circuit current amplification.)

$R_i << R_s$ and $R_o >> R_L$

8.1.3 TRANSCONDUCTANCE AMPLIFIER



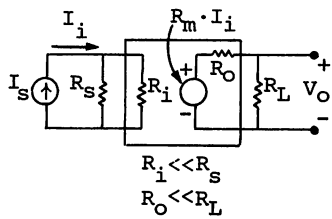
Thevenin's equivalent in its input circuit and a Norton's equivalent in its output circuit.

Output current is proportional to the signal voltage and is independent of R_S and R_L.

G_m (the short circuit mutual or transfer conductance)

$$= \frac{I_o}{V_i} \text{ for } R_L = 0$$

8.1.4 TRANSRESISTANCE AMPLIFIER



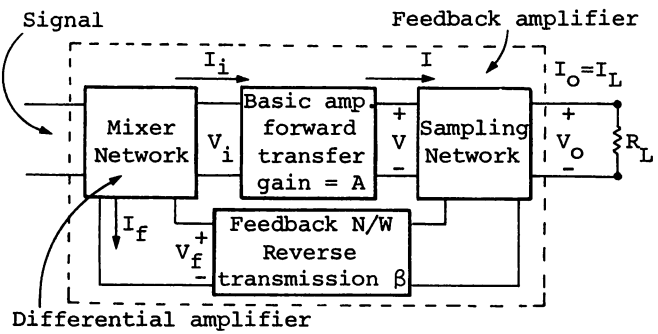
V_o is proportional to the signal current I_s and is independent of R_s and R_L.

$$R_m = \frac{V_o}{I_i} \text{ with } R_L = \infty \quad (R_m = \text{open circuit mutual resistance})$$

8.1.5 IDEAL AMPLIFIER CHARACTERISTICS

	Amplifier type			
Parameter	Voltage	Current	Transconductance	Transresistance
R_i	∞	0	∞	0
R_o	0	∞	∞	0
Transfer Characteristics	$V_o = A_v V_s$	$I_L = A_i I_s$	$I_L = G_m V_s$	$V_o = R_m I_s$

8.2 THE CONCEPT OF "FEEDBACK"



8.2.1 SAMPLING NETWORK

The output voltage is sampled by connecting the feedback network in shunt across the output voltage or node sampling.

Current or loop sampling - The feedback network is connected in series with the output.

8.2.2 TRANSFER RATIO OR GAIN

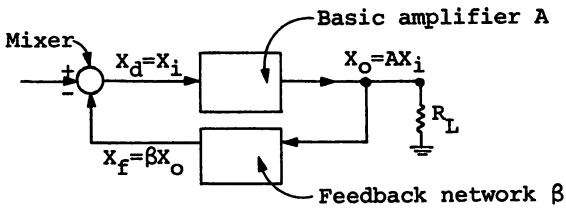
Each of the four quantities A_V, A_I, G_M and R_M is a different type of transfer gain of the basic amplifier without feedback (A).

A_f = The transfer gain with feedback. $= A_{vf}$ or A_{If} or G_{Mf} or R_{Mf}

$$A_{vf} = \frac{V_o}{V_s}, \quad \frac{I_o}{I_s} = A_{If}, \quad \frac{I_o}{V_s} = G_{Mf}, \quad \frac{V_o}{I_s} = R_{Mf}$$

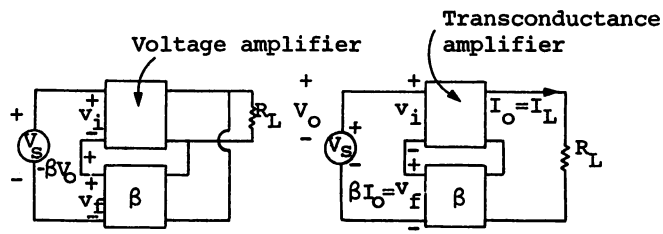
8.3 TRANSFER GAIN WITH FEEDBACK

8.3.1 SINGLE-LOOP FEEDBACK AMPLIFIER



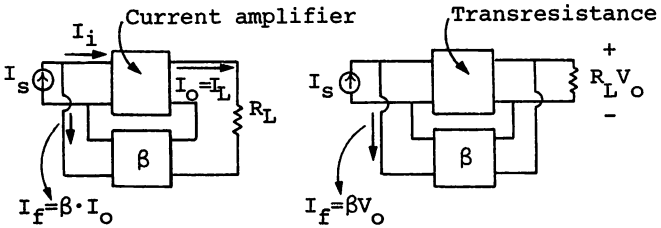
$X_d = X_s - X_f = X_i$ = The difference signal.

8.3.2 FEEDBACK AMPLIFIER TOPOLOGIES



(a) Voltage amplifier with moltage-series feedback

(b) Current-series feedback



(c) Current-shunt feedback

(d) Voltage-shunt feedback

$$\beta \equiv \frac{X_f}{X_o}$$

β is a complex function of the signal frequency and is often a positive or negative real number.

$$A = \frac{X_o}{X_i}$$

$$A_f = \frac{X_o}{X_s} = \frac{A}{1 + \beta A}$$

If $|A_f| < |A|$, the feedback is termed negative; if $|A_f| > |A|$, the feedback is positive, or regenerative.

In the case of negative feedback, the gain of the ideal amplifier is divided by $|1+\beta A|$, which exceeds unity.

Loop gain:

The loop gain = $-A \cdot \beta$ = The return ratio.

The return difference $D = 1 + A\beta$

$$N = \text{dB of feedback} = 20 \log \left| \frac{A_f}{A} \right| = 20 \log \left| \frac{1}{1 + A\beta} \right|$$

8.4 FEATURES OF THE NEGATIVE FEEDBACK AMPLIFIER

Sensitivity - The fractional change in amplification with feedback divided by the fractional change without feedback is the sensitivity of the transfer gain.

$$\frac{\left|dA_f/A_f\right|}{\left|\frac{dA}{A}\right|} = \frac{1}{|1+\beta A|}$$

S = Sensitivity = $\frac{1}{|1+\beta A|}$

Desensitivity = D = $1 + \beta A$.

$A_f = A/D$

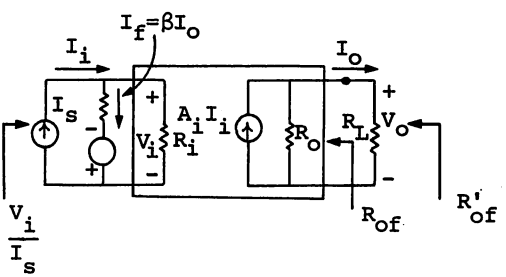
if $|\beta A| >> 1$, $A_f = \frac{A}{1+\beta A}$ $\quad \frac{A}{\beta \cdot A} = \frac{1}{\beta}$

Frequency distortion - If the feedback network does not contain ractive elements, the overall gain is not a function of frequency.

Reduction of noise - The noise introduced in an amplifier is divided by the factor D if feedback is introduced.

8.5 INPUT RESISTANCE

Voltage-series feedback:



$R_{if} = \frac{V_i}{I_s}$

$A_V = \frac{V_o}{V_i} = \frac{A_v R_L}{R_o + R_L}$, $\quad V_o = A_v \cdot I_i \cdot R_i$

$V_s = I_i R_i + \beta V_o$

$R_{if} = \frac{V_s}{I_i} = R_i(1+\beta A_v)$.

$$A_v = \lim_{R_L \to \infty} A_v$$

Current-series feedback:

$$R_{if} = R_i(1+ \beta G_M), \quad G_M = \lim_{R_L \to 0} G_M$$

$$G_M = \frac{I_o}{V_i} = \frac{G_M \cdot R_o}{R_o + R_L}$$

Current-shunt feedback:

$$A_I = \frac{I_o}{I_i} = A_i \cdot R_o/(R_o + R_L)$$

$$I_s = (1 + \beta A_I)I_i$$

$$R_{if} = \frac{V_i}{(1+ \beta A_I)I_i} = \frac{R_i}{1 + \beta A_I}$$

$$A_i = \lim_{R_L \to 0} A_I$$

Voltage-shunt feedback:

$$R_{if} = \frac{R_i}{1 + \beta \cdot R_M}, \quad R_M = \frac{V_o}{V_i} = \frac{R_m \cdot R_L}{R_o + R_L}$$

$$R_m = \lim_{R_L \to \infty} R_M$$

8.6 OUTPUT RESISTANCE

For voltage sampling, $R_{of} < R_o$; whereas, for current sampling, $R_{of} > R_o$.

Voltage series feedback

$$R_{of} = \frac{V}{I} = \frac{R_o}{1 + \beta A_v}, \text{ where } D = 1 + \beta A_v$$

$$R_{of}' = R_o'/1 + \beta A_v , \qquad \text{where } R_o' = R_o \,||\, R_L .$$

Voltage-shunt feedback:

$$R_{of} = \frac{R_o}{1 + \beta R_m}, \quad R_{of}' = R_o'/1 + \beta R_M$$

Current-shunt feedback:

$$R_{of} = \frac{V}{I} = R_o(1+\beta A_i)$$

$$R'_{of} = R_o' \frac{1+\beta A_i}{1+\beta A_I}$$

$$= R_{of} \text{ (for } R_L = \infty,\ A_I = 0 \text{ and } R_o' = R_o).$$

Current-series feedback:

$$R_{of} = R_o(1+\beta G_m) \text{ and } R'_{of} = R_o' \frac{1 + \beta G_m}{1 + \beta G_M}$$

8.7 FEEDBACK AMPLIFIER ANALYSIS

Topology / Characteristic	Voltage shunt	Current shunt	Current series	Voltage series
Feedback signal X_f	Current	Current	Voltage	Voltage
Sample signal X_o	Voltage	Current	Current	Voltage
Input circuit: set†	$V_o = 0$	$I_o = 0$	$I_o = 0$	$V_o = 0$
Output circuit: set†	$V_i = 0$	$V_i = 0$	$I_i = 0$	$I_i = 0$
Signal source	Norton	Norton	Thévenin	Thévenin
$\beta = X_f/X_o$	I_f/V_o	I_f/I_o	V_f/I_o	V_f/V_o
$A = X_o/X_i$	$R_M = V_o/I_i$	$A_I = I_o/I_i$	$G_M = I_o/V_i$	$A_v = V_o/V_i$
$D = 1 + \beta A$	$1 + \beta R_M$	$1 + \beta A_I$	$1 + \beta G_M$	$1 + \beta A_v$
A_f	R_M/D	A_I/D	G_M/D	A_v/D
R_{if}	R_i/D	R_i/D	R_iD	R_iD
R_{of}	$\frac{R_o}{1 + \beta R_m}$	$R_o(1 + \beta A_i)$	$R_o(1 + \beta G_m)$	$\frac{R_o}{1 + \beta A_v}$
$R'_{of} = R_{of} \,\|\|\, R_L$	$\frac{R_o'}{D}$	$R_o' \frac{1 + \beta A_i}{D}$	$R_o' \frac{1 + \beta G_m}{D}$	$\frac{R_o'}{D}$

Analysis of a feedback amplifier:

Identify the topology - The input loop is defined as the mesh containing the applied signal voltage V_s and either (a) the base-to-emitter region of the first BJT, or (b) the gate-to-source region of the first FET, or (c) the section between the two inputs of a differential amplifier.

Mixing - There is a series mixing in the input circuit if there is a circuit compoment y in series with V_s and if y is connected to the output. If this is true, the voltage across y is the feedback signal $X_f = V_f$.

If this is not true, test for shunt comparison. Shunt mixing is present if the feedback signal subtracts from the applied excitation as a current at the input node.

Type of sampling:

A) Set $V_o = 0$ (i.e., set $R_L = 0$). If X_f becomes zero, the original system exhibited voltage sampling.

B) Set $I_o = 0$. If X_f becomes zero, current sampling was present in the original amplifier.

The amplifier without feedback - The amplifier configuration without providing feedback but with taking the loading of β network into account is obtained by applying following rules.

To find the input circuit:

A) Set $V_o = 0$ for voltage sampling. (i.e., short-circuit the output node)

B) Set $I_o = 0$ for current sampling. (i.e., open-circuit the output loop)

To find the output circuit :

A) Set $V_i = 0$ for shunt comparison.

B) Set $I_i = 0$ for series comparison. In other words, open-circuit the input loop

Outline of analysis - To find A_f, R_{if} and R_{of} the following steps are carried out:

A) Find out the topology first. It will determine whether X_f is a voltage or a current. The same applies to X_o.

B) Using the above rules, draw the basic amplifier circuit without feedback.

C) If X_f is a voltage, use a Thevenin's source; use Norton's source if X_f is a current.

D) Substitute the proper model for each active device (h-parameter model).

E) Indicate X_f and X_o on the circuit obtained by steps B, C, and D. Calculate $\beta = \frac{X_f}{X_o}$

F) Apply KVL and KCL to the equivalent circuit obtained after step D, to find A.

G) Calculate D, A_f, R_{if}, R_{of} and R'_{of} from A and B.

CHAPTER 9

FREQUENCY RESPONSE OF AMPLIFIERS

9.1 FREQUENCY DISTORTION

A plot of gain (phase) versus frequency of an amplifier is called the amplitude (phase) frequency-response characteristic.

If the amplification A is independent of frequency, and if the phase shift θ is proportional to frequency (or is zero), then the amplifier will preserve the form of the input signal, although the signal will be shifted in time by an amount θ/ω.

Frequency-response characteristics:

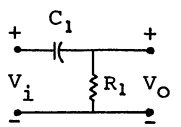
A) Low-frequency region: The amplifier behaves like a simple high-pass circuit.

B) Mid-band frequency: Amplification and delay is quite constant. The gain is normalized to unity.

C) High-frequency region: The circuit behaves like a low-pass network.

Low and high-frequency response:

Low-frequency response:



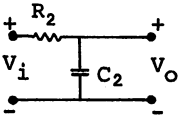
The low-frequency region is like a simple high-pass circuit.

$$V_o = \frac{R_1}{R_1 + \frac{1}{SC_1}}, \quad V_i = \frac{S}{S + \frac{1}{R_1C_1}} V_i$$

$$|A_L(f)| = \frac{1}{1-j(f_L/f)}, \quad f_L = \frac{1}{2\pi R_1C_1}, \quad \theta_L = \text{arc tan } \frac{f_L}{f}$$

The low-3dB-frequency: At this frequency, the gain has fallen to 0.707 times its mid-band value A_o; $f = f_L$ is the low-3dB frequency.

High-frequency response:



$$V_o = \frac{\frac{1}{SC_2}}{R_2 + \frac{1}{SC_2}} \qquad V_i = \frac{1}{1 + SR_2C_2} V_i$$

$$|A_H(f)| = 1/\sqrt{1+(f/f_H)^2} \qquad \theta_H = -\text{arc tan } \frac{f}{f_H}$$

$$f_H = 1/2\pi R_2C_2$$

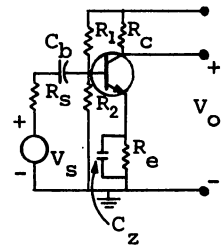
The high-3dB frequency: At $f = f_H$, the gain is reduced to $1/\sqrt{2}$ times its mid-band value, this is called the high-3dB frequency.

Bandwidth: B.W. = frequency range from f_L to f_H.

9.2 THE EFFECT OF COUPLING AND EMITTER BYPASS CAPACITORS ON LOW-FREQUENCY RESPONSE

An emitter resistance R_e is used for self-bias in an

amplifier and to avoid degeneration; C_Z is used to bypass R'_e.



$$V_o = -I_b h_{fe} R_c = \frac{-V_s \cdot h_{fe} \cdot R_c}{R_s + h_{ie} + Z_b + Z'_e}$$

$$Z_b = \frac{1}{j\omega c_b} \quad \text{and} \quad Z'_e = (1+h_{fe}) \frac{R_e}{1+j\omega C_z \cdot R_e}$$

$$j\omega(Z_b + Z'_e) = \frac{1}{C_b} + \frac{1+h_{fe}}{C_Z} = \frac{1}{C_1}$$

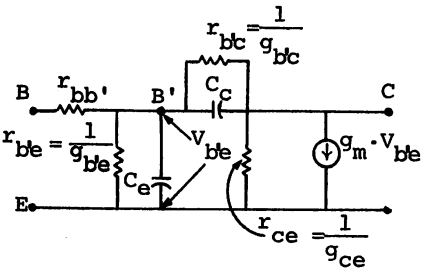
$$C_1 = C_b + \frac{C_Z}{1+h_{fe}}$$

$$A_{vs} = \frac{V_o}{V_s} = \frac{-h_{fe} R_c}{R_s + h_{ie}} \cdot \frac{1}{1 - j/\omega c_1 (R_s + h_{ie})}$$

$$A_o = \text{mid-band gain} = \frac{-h_{fe} \cdot R_c}{R_s + h_{ie}}, \quad \frac{A_{vs}}{A_o} = \frac{1}{1-j(f_L/f)}$$

Low-3dB freq. $f_L = 1/2\pi C_1 (R_s + h_{ie})$ $(\text{at } f_L,\ R_s + h_{ie} = R_1)$

9.3 THE HYBRID-π TRANSISTOR MODEL AT HIGH FREQUENCIES

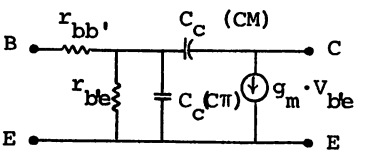


$C_c = C_{b'c}$ is the measured C_B ouptut capacitance with the input open ($I_E = 0$). (C_c is the transition capacitance, which varies as V_{CB}^{-n}, where n is $\frac{1}{2}$ or $\frac{1}{3}$). $C_e = C_{De} + C_{Te}$, where C_{De} is the emitter diffusion capacitance and C_{Te} is emitter-junction capacitance.

The diffusion capacitance:

$$C_{De} = g_m \frac{W^2}{2D_B}$$ (D_B = the diffusion constant for minority carriers)

Simplified model:



Variations of Hybrid-π barameters:

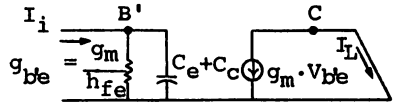
Dependence of parameters upon current, voltage and temperature

Variation with increasing:

Parameter	$\lvert I_c \rvert$	$\lvert V_{CE} \rvert$	T
g_m	$\lvert I_C \rvert$	Independent	1/T
$r_{bb'}$	Decreases		Increases
$r_{b'e}$	$1/\lvert I_C \rvert$	Increases	Increases
C_e	$\lvert I_C \rvert$	Decreases	
C_c	Independent	Decreases	Independent
h_{fe}		Increases	Increases
h_{ie}	$1/\lvert I_C \rvert$	Increases	Increases

9.4 THE C-E SHORT-CIRCUIT CURRENT GAIN

Approximate equivalent circuit:



$$I_L = -g_m \quad V_{b'e}$$

$$V_{b'e} = I_i/g_{b'e} + j\,\omega(C_e+C_c)$$

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{(g_{b'e}+j\,\omega[C_e+C_c])} = \frac{-h_{fe}}{1+j(f/f_\beta)}$$

$$f_\beta = \frac{g_{b'e}}{2\pi(C_e+C_c)} = \frac{1}{h_{fe}} \frac{g_m}{2\pi(C_e+C_c)}$$

At $f = f_\beta$, $|A_i|$ is equal to $1/\sqrt{2} = 0.707$ of its low-frequency value, h_{fe}.

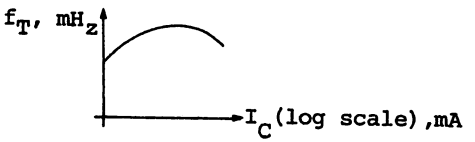
B.W. = The frequency range up to f_β.

The parameter f_T:

f_T is the frequency at which the short-circuit common-emitter current gain attains unit magnitude.

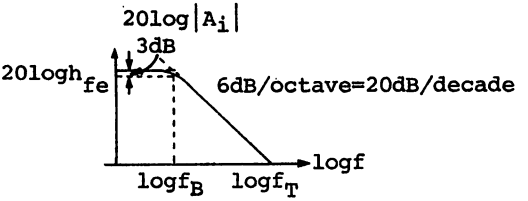
$$f_T \approx h_{fe} \cdot f_\beta = \frac{g_m}{2\pi(C_e+C_c)} \approx \frac{g_m}{2\pi \cdot C_e}$$

Variation of f_T on collector current:



f_T also represents the short-circuit current gain-bandwidth product.

The plot of the short-circuit CE current gain versus the frequency:

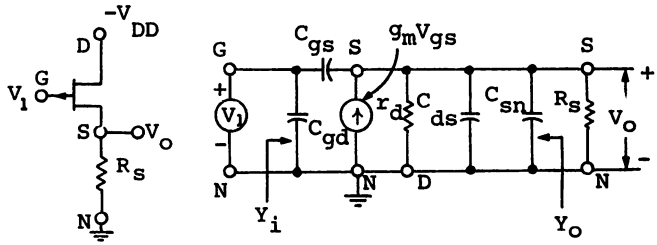


At f_T (the highest frequency of interest),

$$\frac{\omega C_c}{g_m} = \frac{2\pi \cdot f_T\ C_c}{g_m} = \frac{C_c}{C_e+C_c} \cong 0.03$$

9.5 THE COMMON-DRAIN AMPLIFIER AT HIGH FREQUENCIES

The source-follower and its small-signal high-frequency equivalent circuit:



$$A_v = \text{The voltage gain} = \frac{(g_m + j\omega C_{gs})R_s}{1+(g_m+g_d+j\omega C_T)R_s}$$

$$C_T = C_{gs} + C_{ds} + C_{sn}$$

$$A_v(\text{at low frequency}) \approx \frac{g_m \cdot R_s}{1+(g_m+g_d)R_s} \approx \frac{g_m}{g_m+g_d}$$

$$= \frac{\mu}{1+\mu}$$

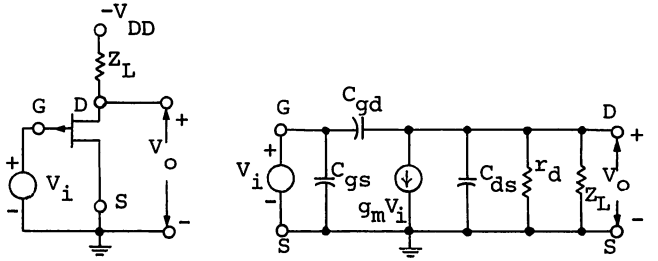
Input and output admittance:

$$y_i = j\omega C_{gd} + j\omega C_{gs}(1-A_v) \approx j\omega C_{gd}$$

$$y_o = g_m + g_d + j\omega C_T$$

$$R_o \text{ (at low frequency)} = 1/g_m + g_d \approx 1/g_m$$

9.6 THE COMMON-SOURCE AMPLIFIER AT HIGH FREQUENCIES



$$I = -g_m \cdot V_i + V_i \cdot y_{gd}$$

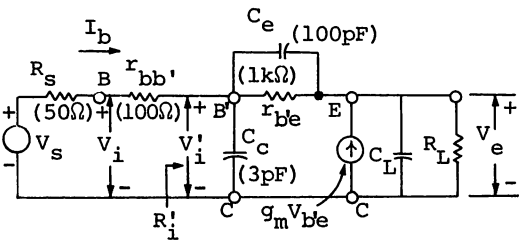
The amplification is $A_v = \frac{V_o}{V_i} = \frac{I \cdot Z}{V_i} = \frac{-g_m + y_{gd}}{y_L + g_d + y_{ds} + y_{gd}}$

$$A_v \text{ (at low frequencies)} = \frac{-g_m}{y_L + g_d} = \frac{-g_m \cdot r_d \cdot Z_L}{r_d + Z_L} = -g_m \cdot Z'_L$$

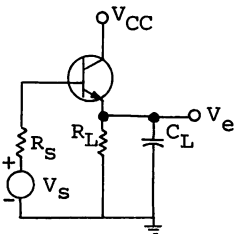
The input admittance is

$$y_i = y_{gs} + (1-A_v)y_{gd} = G_i + j\omega C_i \approx j\omega C_{gd}$$

9.7 THE EMITTER-FOLLOWER AMPLIFIER AT HIGH FREQUENCIES



High-frequency equivalent circuit



Emitter-follower

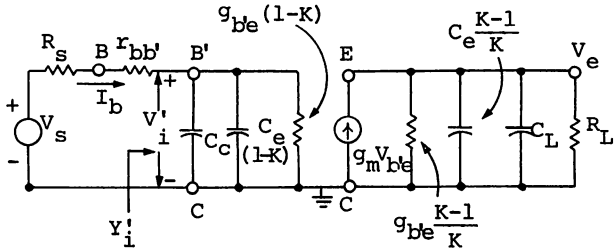


Fig: Equivalent circuit using Miller's theorem

The nodal equations at the nodes of B' and E are:

$$G'_s V_s = [G'_s + g_{b'e} + s(C_c+C_e)]v'_i - (g_{b'e} + sC_e)V_e$$

$$0 = -(g + sC_e)V'_i + [g + \frac{1}{R_L} + s(C_e+C_L)]V_e$$

$$G'_s = 1/R_s + r_{bb'} \quad \text{and} \quad g = g_m + g_{b'e}$$

Single pole solution:

$$K = V_e/V'_i$$

$$V_e = \frac{g_m \cdot V_{b'e}}{\frac{1}{R_L} + j\omega C_L} = \frac{g_m \cdot R_L(V'_i - V_e)}{1+j\omega C_L R_L} \quad \text{(for K=1)}$$

$$K = \frac{K_o}{1 + jf/f_H}, \quad K_o = \frac{g_m \cdot R_L}{1 + g_m \cdot R_L} \approx 1.$$

$$f_H = \frac{1 + g_m \cdot R_L}{2\pi \cdot C_L \cdot R_L} \approx \frac{g_m}{2\pi C_L} = \frac{f_T \cdot C_e}{C_L}$$

Input admittance:

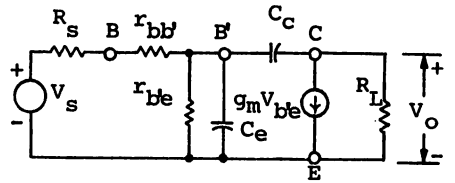
$$Y'_i = \frac{I_b}{V'_i} = j\omega[C_c + (1-K)C_e] + (1-K)g_{b'e}$$

$$Y'_i = j2\pi f \cdot C_c + (g_{b'e} + j2\pi \cdot f \cdot C_e)\frac{1 - K_o + jf/f_H}{1 + jf/f_H}$$

$$Y'_i = j2\pi f \cdot C_c + j\, g_{b'e} \cdot f/f_H - 2\pi \cdot f^2 \frac{C_e}{f_H}$$

9.8 SINGLE-STAGE CE TRANSISTOR AMPLIFIER RESPONSE

Equivalent circuit:



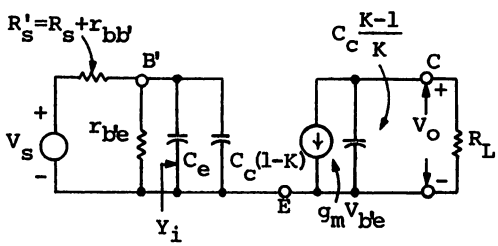
The transfer function:

$$\frac{V_o}{V_s} = \frac{-G_s' \cdot R_L(g_m - sC_c)}{s^2 C_e \cdot C_c \cdot R_L + s[C_e + C_c + C_c R_L(g_m + g_{b'e} + G_s')] + G_s'}$$

The transfer function is of the form

$$A_{vs} = \frac{V_o}{V_s} = \frac{K_1(s-s_0)}{(s-s_1)(s-s_2)}$$

Approximate analysis:



After application of Miller's theorem

$K = \frac{V_{ce}}{V_{b'e}}$, for $|K| >> 1$. Also the output capacitance is C_c and the output time constant is $C_c \cdot R_L$.

$K = -g_m \cdot R_L$ (neglecting C_c)

Input capacitance $C = C_e + C_c(1 + g_m \cdot R_L)$

Input loop resistance = $R = R_s' \parallel r_{b'e}$

$$A_{vs} = v_o/v_s = (-g_m \cdot R_L \cdot G_s')/(G_s' + g_{b'e} + sC)$$

$$A_{vs} = \frac{A_{vso}}{1 + j\, f/f_H}$$

The high 3-dB frequency = $f_H = \frac{G_s' + g_{b'e}}{2\pi C} = \frac{1}{2\pi R \cdot C}$

$$|A_{vs}| = \frac{|A_{vso}|}{[1 + (f/f_H)^2]^{\frac{1}{2}}}, \quad \theta_1 = -\pi - \arctan f/f_H$$

The ESSENTIALS of ELECTRONICS II

Staff of Research and Education Association,
Dr. M. Fogiel, Director

This book is a continuation of *"THE ESSENTIALS OF ELECTRONICS I"* and begins with Chapter 10. It covers the usual course outline of Electronics II. Earlier/basic topics are covered in *"THE ESSENTIALS OF ELECTRONICS I"*.

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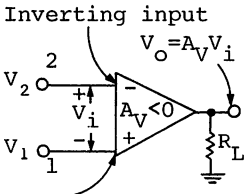
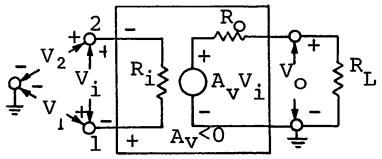
CHAPTER 10

OPERATIONAL AMPLIFIERS

10.1 THE BASIC OPERATIONAL AMPLIFIER



Basic opamp



Low-frequency model of opamp

Ideal op amp:

A) $R_i = \infty$

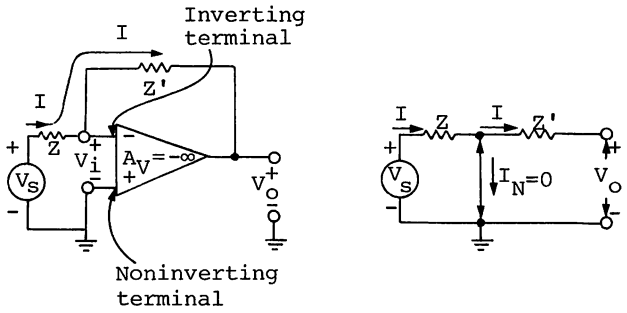
B) $R_o = 0$

C) $A_v = -\infty$

D) B.W. = ∞

E) $V_o = 0$ when $V_1 = V_2$, independent of the magnitude of V_1

F) no drift of characteristics

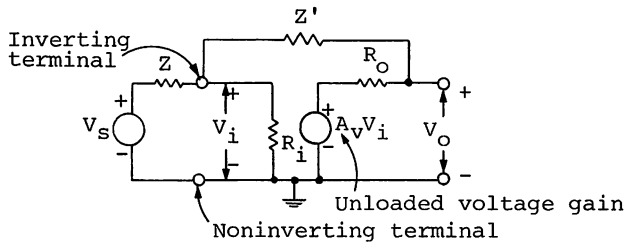


Ideal op amp with feedback impedances

This is the basic inverting circuit. This topology represents voltage-shunt feedback.

$$A_{vf} = \text{voltage gain with feedback} = \frac{-Z'}{Z}$$

Inverting operational amplifier:



Small signal model

For a small-signal model, $|A_v| \neq \infty$, $R_i \neq \infty$ and $R_o \neq 0$.

$$A_{vf} = -y/y' - \left(\frac{1}{A_v}\right)(y'+y+y_i)$$

(where the y's are the admittances)

$$-A_v = \frac{V_o}{V_i} \text{ (with Z')} = \frac{A_v + R_o y'}{1 + R_o y'}$$

Non-inverting op amp:

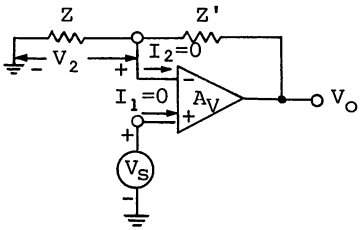
The configuration is that of a voltage-series feedback amplifier, with the feedback voltage, v_f, equal to v_2.

The feedback factor $\beta = \frac{V_2}{V_o} = \frac{Z}{Z+Z'}$ $(I_2 = 0)$

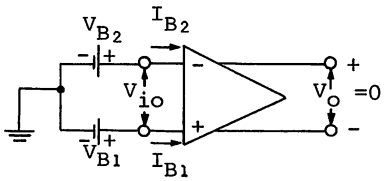
If $A_v \beta >> 1$, then

$$A_{vf} \approx 1/\beta = \frac{Z+Z'}{Z} = 1 + \frac{Z'}{Z}$$

Configuration:



10.2 OFFSET ERROR VOLTAGES AND CURRENTS



Input bias currents I_{B_1} and I_{B_2} and offset voltage V_{io}.

The input offset current is the difference between the input currents entering the input terminals of a balanced amplifier. In the figure above,

$$I_{io} = I_{B_1} - I_{B_2} \qquad (\text{when } V_o = 0)$$

Input offset current drift - This drift is described by the ratio $\frac{\Delta V_{io}}{\Delta T}$,where

ΔV_{io} = the change of input offset voltage

and ΔT = change in temperature.

Input offset voltage - When applied to the input terminals, this voltage will balance the amplifier.

Input offset voltage drift:

$$\frac{\Delta V_{io}}{\Delta T}$$

ΔV_{io} = change of input offset voltage.

Output offset voltage - This voltage marks the difference between the dc voltages measured at the output terminals on grounding the two input terminals.

Input common mode range - This is the range of the common mode input signal for which the differential amplifier remains linear.

Input differential range - This range is the maximum difference signal that can safely be applied to the op amp input terminals.

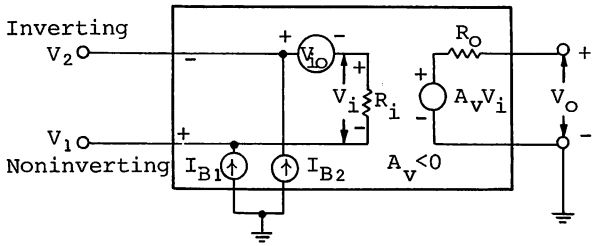
Output voltage range - This is the maximum output swing that can be obtained without significant distortion at a specified load resistance.

Full-power bandwidth - This bandwidth is the maximum frequency at which a sinusoid whose size is the output voltage range is obtained.

Slew rate - This is the time rate of change of the closed-loop amplifier output voltage under large signal conditions.

The model of an op amp and balancing techniques:

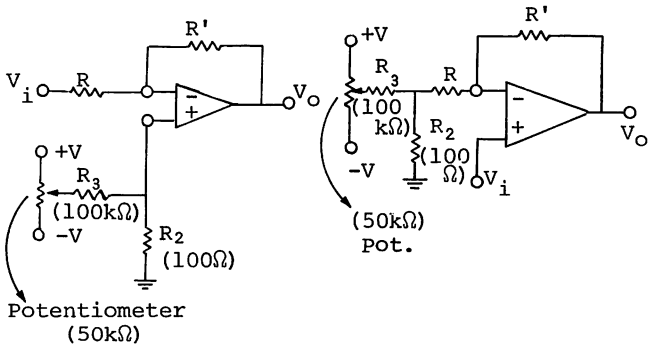
Model:



Universal balancing technique:

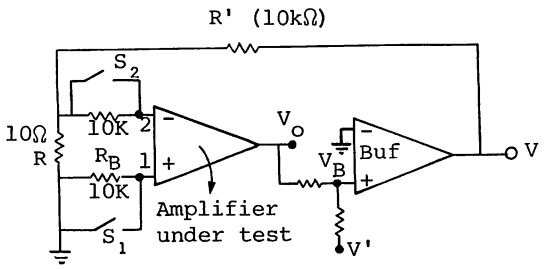
It is necessary to apply a small dc voltage in the input to bring the d output voltage to zero.

The following circuit supplies a small voltage in a series where, the non-inverting terminal is in the range $\pm V\left[\frac{R_2}{R_2+R_3}\right]$ = ±15mV, if ±15 V supplies are used.



10.3 MEASUREMENT OF OPERATIONAL AMPLIFIER PARAMETERS

Input offset voltage V_{io}:



Set V' = 0 to get $V_o = 0$. The close s_1 and s_2.

If $V_o = 0$, then $V_i = 0$, and V_{io} appears between the inverting and non-inverting terminals.

$$V = \frac{V_{io}}{R}(R+R') = 1001\, V_{io} \approx 10^3 V_{io} \equiv V_3.$$

From the meter reading V_3 in volts, we get V_{io} in mv.

Power supply rejection ratio $= \frac{\Delta V_{io}}{\Delta V_{ce}}$ (ΔV_{io} and ΔV_{ce} the difference in the two input offset voltages)

Input bias current:

S_1 and S_2 are open and closed, respectively, and V' = 0.

Voltage across $R = V_{io} - R_B \cdot I_{B_1}$ and $V = \frac{R+R'}{R}(V_{io} - R_B \cdot I_{B_1})$

$$\approx 10^3 (V_{io} - 10^4 I_{B_1}) \equiv V_4$$

$$-I_{B_1} = (V_4 - V_3)10^{-7}A = 100(V_4 - V_3)mA$$

Open s_2 and close s_1; V' = 0 and we get I_{B_2}.

Bias current $I_B = \frac{1}{2}(I_{B_1} + I_{B_2})$ and $I_{io}(\text{offset}) = I_{B_1} - I_{B_2}$.

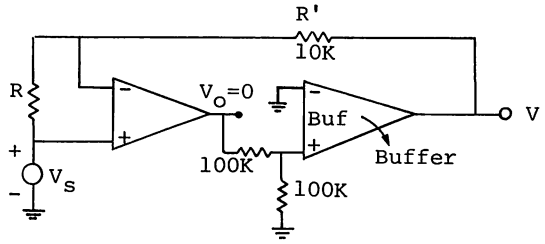
Open-loop differential voltage gain $A_v = A_d$:

S_1 and S_2 are closed, and V' is set to the output voltage = -10V then, V_o = -V' = 10v.

$$V = \frac{R+R'}{R}(V_{io}+V_i) \approx 10^3\left(V_{io}+\frac{V_o}{A_v}\right) \equiv V_5$$

$$A_v = \frac{10^3 \cdot V_o}{V_5 - V_3} = 10^4/V_5 - V_3$$

If we want to know the voltage gain A_v when there is a load, it is necessary to place R_L between V_o and the ground.



Close S_1 and S_2 ; V' = 0; apply signal v_s.

$$V_o = A_d \cdot V_d + A_c \cdot V_c = 0$$

$$V_1 = V_s \quad \text{and} \quad V_2 = V_s \cdot \frac{R'}{R+R'} + V \cdot \frac{R}{R+R'} \cong V_s + \frac{V \cdot R}{R'}$$

$$V_d = V_1 - V_2 - V_{io} = \frac{-R}{R'}(V+V_3)$$

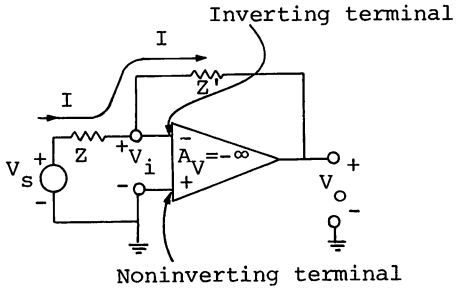
$$V_c = V_s + (VR/2R')$$

$$-A_d \frac{R}{R'}(V+V_3) + A_c\left[V_s + \frac{V \cdot R}{2R'}\right] = 0$$

If the measured value of V is V_6, then

$$\rho \cdot \frac{R}{R'}(V_6+V_3) = v_s$$

Slew rate - The slew rate is the maximum rate of change of the output voltage when supplying the rated output.

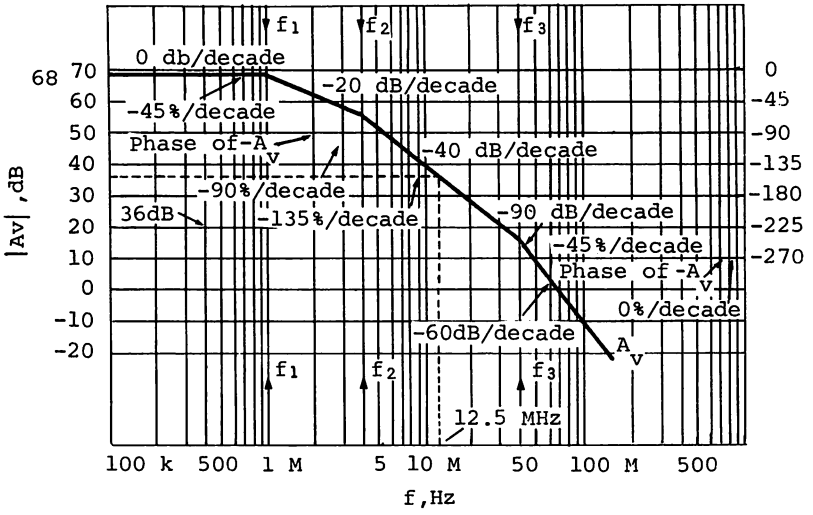


For a single-ended input amplifier, adjust Z = R = 1K and Z' = R' = 10KΩ.

V_s is a high-frequency square-wave. Its slopes are measured with respect to the lines of the leading and trailing edges of the output signal.

The slower of the two is the slew rate.

Frequency response of the op amp:

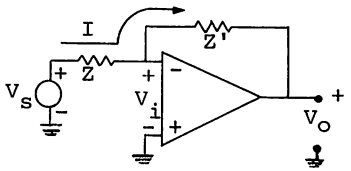


CHAPTER 11

OPERATIONAL AMPLIFIER SYSTEMS

11.1 BASIC OPERATIONAL AMPLIFIER APPLICATIONS

11.1.1 SIGN CHANGER, OR INVERTER



If $Z = Z'$, then $A_{vf} = \frac{V_o}{V_s} = \frac{-Z'}{Z} = -1$.

The sign of the input signal is changed at the output.

The circuit acts as a phase inverter.

11.1.2 SCALE CHANGER

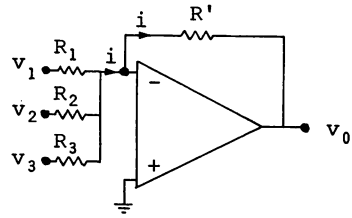
If the ratio $\frac{Z'}{Z} = K$ (a real constant), then $A_{vf} = -K$.

The scale has been multiplied by the factor -K.

11.1.3 PHASE SHIFTER

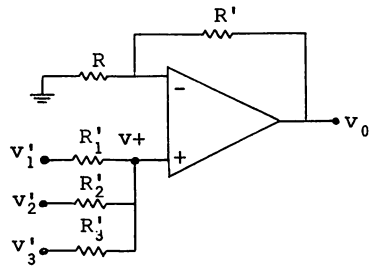
If Z and Z' are equal in magnitude and differ in angle, then the op amp shifts the phase of a sinusoidal input voltage.

11.1.4 ADDER



$$v_o = \frac{-R'}{R}(v_1+v_2+v_3), \text{ if } R_1 = R_2 = R_3 = R$$

11.1.5 NON-INVERTING ADDER



$$v_o = \left(1 + \frac{R'}{R}\right) v_+$$

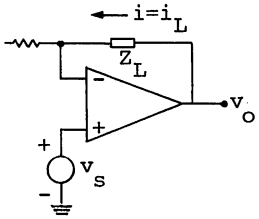
For n equal to resistors, each of value R'_2

$$\frac{R'_{p_2}}{R'_2 + R'_{p_2}} = \frac{R'_2 \div (n-1)}{R'_2 + [R'_2 \div (n-1)]} = \frac{1}{n}$$

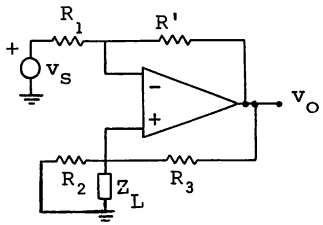
$$v_+ = \frac{1}{n}(v'_1 + v'_2 \ldots).$$

$$R'_{p_2} = R'_1 \,||\, R'_3 \,||\, R'_4 \ldots ||\, R'_n$$

11.1.6 VOLTAGE-TO-CURRENT CONVERTER (TRANSCONDUCTANCE AMPLIFIER)



For a floating load



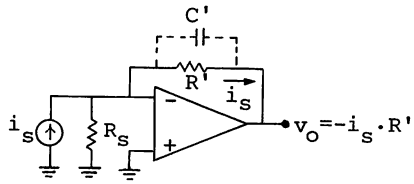
A grounded load

Floating load (neither side is grounded):

The current in $Z_L = i_L = \frac{v_{s(t)}}{R_1}$.

Grounded load: $i_L(t) = -\frac{v_{s(t)}}{R_2}$

11.1.7 CURRENT-TO-VOLTAGE CONVERTER

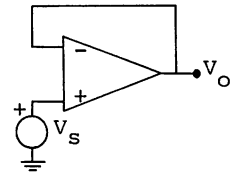


C' is used to reduce the high-frequency noise as well as the possibility of oscillations.

$$v_o = -i_s R'$$

The circuit acts like an ammeter with zero voltage across the meter.

11.1.8 D.C. VOLTAGE FOLLOWER

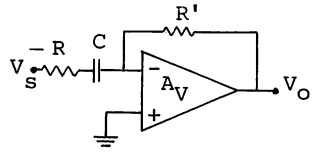


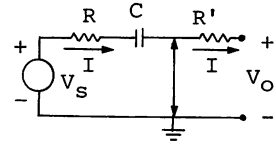
$V_o = V_s$ (because the inputs are tied (virtually) together)

The follower has a high input resistance and a low output resistance.

11.2 AC-COUPLED AMPLIFIER

This is used for amplifying an ac signal, while any dc signal is to be blocked.





Equivalent circuit

$$V_o = -IR' = \frac{-V_s}{R + \frac{1}{sC}} R'$$

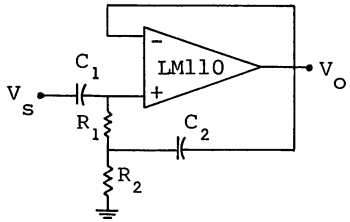
$$A_{vf} = \frac{V_o}{V_s} = \frac{-R'}{R} \quad \frac{s}{s + \frac{1}{RC}}$$

f_L = low 3-dB frequency = $1/2\pi$ RC

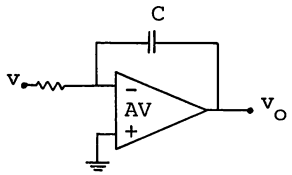
AC voltage follower:

This follower is used to connect a signal source with

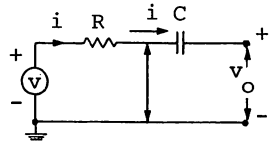
high internal source resistance to a load of low impedance, which may be capacitive.



Analog integration and differentiation:



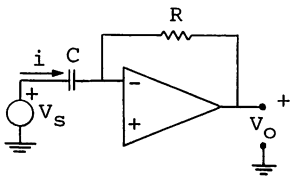
Integrator



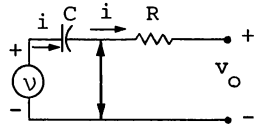
Equivalent circuit

$$v_o = \frac{-1}{C}\int i\,dt = \frac{-1}{RC}\int v\,dt$$

If the input voltage is constant, v = V, then the output will be a ramp, $v_o = \frac{-Vt}{RC}$.



Differentiator



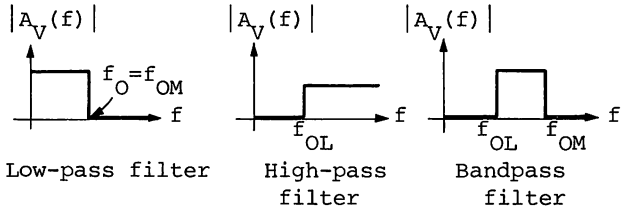
Equivalent circuit

$$v_o = -R_i = -RC\frac{dv}{dt}$$

If the input signal is $v = \sin \omega t$, then the output will be $v_o = -RC\omega \cos \omega t$. This results in amplification of the high-frequency components of amplifier noise, and the noise output may completely mask the differentiated signal.

11.3 ACTIVE FILTERS

11.3.1 IDEAL FILTERS



An approximation for an ideal low-pass filter is:

$$\frac{A_v(s)}{A_{vo}} = \frac{1}{P_n(s)}$$

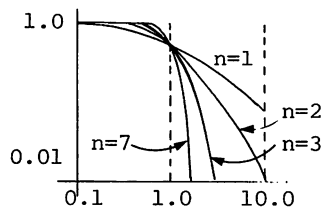
where $P_n(s)$ is a polynomial in the variable s with zeros in the left-hand plane.

11.3.2 BUTTERWORTH FILTER

$P_n(s) = B_n(s)$, known as the "Butterworth polynomial"

$$|B_n(\omega)| = \left[1 + \left(\frac{\omega}{\omega_o}\right)^{2n}\right]^{\frac{1}{2}}$$

Butterworth low-pass filter response:



The transfer function is

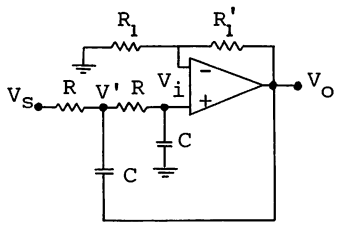
$$\frac{A_v(s)}{A_{vo}} = \frac{1}{(s/\omega_o)^2 + 2K(s/\omega_o) + 1}$$

where $\omega_o = 2\pi f_o$ = High-frequency 3-dB point.

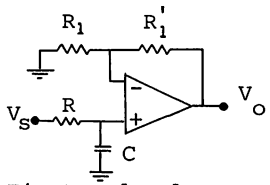
This represents a second-order filter.

For the first-order filter, $\frac{A_v(s)}{A_{vo}} = \frac{1}{\frac{s}{\omega_o} + 1}$

Circuit



Second-order low-pass section



First-order low-pass section

Mid-band gain of op amp,

$$A_{vo} = \frac{V_o}{V_i} = \frac{R_1+R_1'}{R_1}$$

$$\frac{A_v(s)}{A_{vo}} = 1/[(RC_s)^2 + (3-A_{vo})RCs + 1]$$

obtained by applying KCL to node V'.

$$\omega_o = \frac{1}{RC} \quad \text{and} \quad 2K = 3 - A_{vo}\ldots$$

by comparing the coefficients of s^2 in $\frac{A_v(s)}{A_{vo}}$ and typical second-order transfer function.

Even-order Butterworth filters are synthesized by cascading second-orders prototypes such as those shown above and choosing A_{vo} of each op amp such that $A_{vo} = 3 - 2K$.

Normalized Butterworth polynomials:

n	Factors of $B_n(s)$
1	$(s+1)$
2	$(s^2+1.414\ s+1)$
3	$(s+1)(s^2+s+1)$
4	$(s^2+0.765s+1)(s^2+1.848s+1)$
5	$(s+1)(s^2+0.618s+1)(s^2+1.618s+1)$

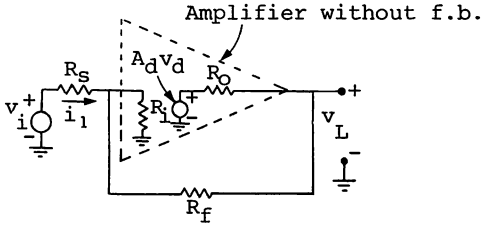
Odd-order filters - Cascade the first-order filter with the second order.

CHAPTER 12

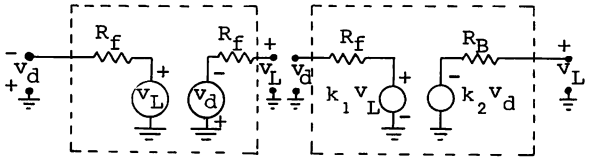
FEEDBACK AND FREQUENCY COMPENSATION OF OP AMPS

12.1 BASIC CONCEPTS OF FEEDBACK

Standard inverting configuration:



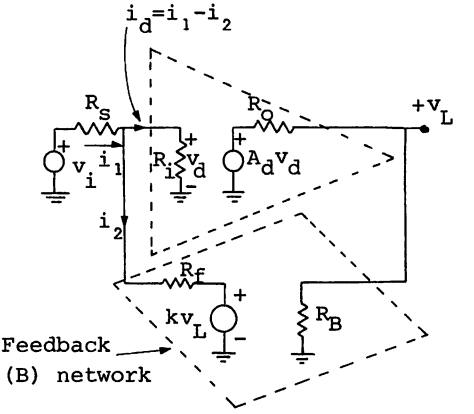
(a) Configuration



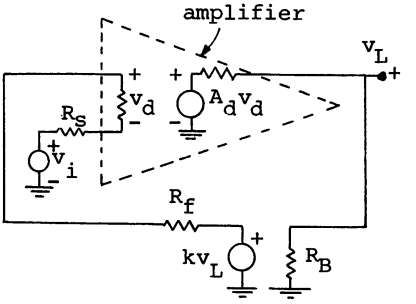
(b) f.b. network equivalent ck.

(c) General equivalent circuit

Current-differencing negative feedback circuit:



(a) Current-differencing -ve - feedback ckt.



(b) Voltage-differencing
-ve f.b. circuit

Gain of a feedback amplifier with current differencing:

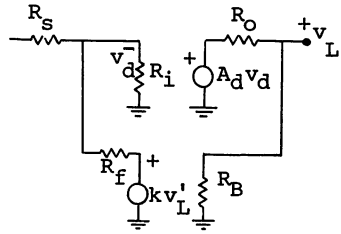
$$i_1 = \frac{v_i + v_d}{R_s}, \quad i_2 = \frac{-v_d + K \cdot v_L}{R_f}, \quad i_d = \frac{-v_d}{R_i}$$

$$v_L \cong -(v_i A_d \div R_s)(R_s \parallel R_f) \div [1 + (A_d \cdot K/R_f)(R_s \parallel R_f)]$$

$$\cong -[R_f \div (K \cdot R_s)]v_i \quad \ldots \quad \text{(For inverting configuration } K = 1\text{)}$$

Loop-gain T of the amplifier:

$$\frac{-A_d K}{R_f}\,(R_s // R_f)$$



Circuit used to calculate T and A_o:

$$T = \left.\frac{v_L}{v'_i}\right|_{v_i=0} = \frac{v_L}{v_d}\,\frac{v_d}{i_d}\,\frac{i_d}{v'_L}$$

Open loop gain, or gain without feedback A_o:

$$A_o = \left.\frac{v_L}{v_i}\right|_{v_L=0} = \frac{-A_d}{R_s}\,(R_s \| R_f)$$

Overall gain:

$$A_v = \frac{v_L}{v_i} = \frac{A_o}{1-T}$$

For voltage-differencing circuit:

$$T \cong -A_d \cdot K$$

$$A_o \approx A_d$$

$$v_L \approx v_i A_d/(1+A_d K)$$

The loop gain T:

The loop gain controls the "amount" of feedback present in a circuit.

If T = 0 (K=0), there is no feedback.

When T >>1, the gain of an amplifier with feedback approaches $A_v = v_L/v_i = -(R_f/KR_s)$ for the current-differencing configuration, and $A_v = \frac{1}{K}$ for the voltage-differencing configuration. (These amplifiers are shown in the diagram above.) We note that in both cases the gain with feedback is more or less independent of the amplifer gain, A_d. Consequently, the amplifier employing feedback is much more stable against variations in temperature and other parameters as the loop gain increases.

The feedback also has the effect of decreasing the gain from A_o (without feedback) to $\frac{A_o}{(1-T)}$.

Feedback amplifiers and the sensitivity function:

Sensitivity function: $\int_{A_o}^{A_v} = \frac{dA_v/A_v}{dA_o/A_o}$

$$\int_{A_o}^{A_v} = 1/(1 - T)$$

12.2 FREQUENCY RESPONSE OF A FEEDBACK AMPLIFIER

Bandwidth and Gain-bandwidth Product:

For current-differencing negative feedback Amplifier:

$$A_v = \frac{A_o}{1 - T}$$

Single-pole amplifier:

$$A_d = \frac{A_{dm}}{1+(s/\omega_1)} \quad \cdots \quad A_{dm} = \text{gain at low frequency}$$

$$T = \frac{-T_m}{1+\left(\frac{s}{\omega_1}\right)}, \quad T_m = \frac{A_{dm} \cdot K(R_s \| R_f)}{R_f}, \quad A_o = \frac{-A_{om}}{1+\left(\frac{s}{\omega_1}\right)},$$

$$A_{om} = \frac{A_{dm}(R_s \| R_f)}{R_s}$$

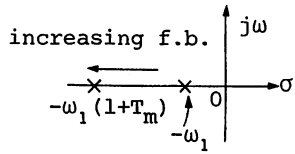
$$A_v = \frac{-A_{om}}{1+T_m}\left(\frac{1}{1+\frac{s}{\omega_1}(1+T_m)}\right)$$

A pole is located at $s = -\omega_1(1 + T_m)$

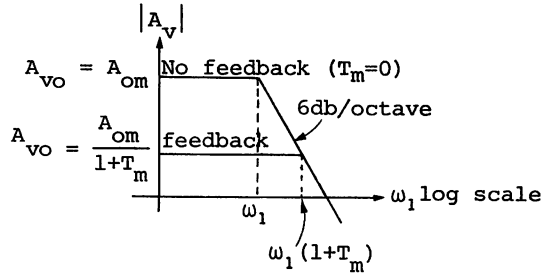
f_n(upper 3-dB frequency) $= f_1(1 + T_m)$

$G \times (B.W.) = \left[A_{v(f=0)}\right] \cdot f_n = A_{om} \cdot f_1$(A constant, independent of feedback)

Characteristic:



(a) locus of pole motion



(b) Gain versus frequency.

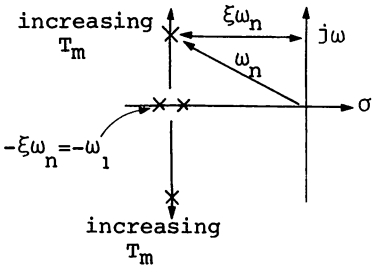
Double-pole amplifier:

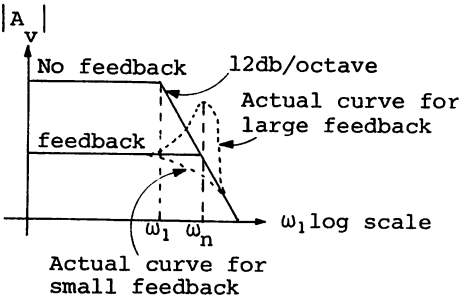
$$A_d(s) = \frac{A_{dm}}{\left(1 + \frac{s}{\omega_1}\right)^2}, \quad T = \frac{-T_m}{\left(1 + \frac{s}{\omega_1}\right)^2}$$

$$A_o = \frac{-A_{om}}{\left(1 + \frac{s}{\omega_1}\right)^2}, \qquad A_v(s) = \frac{-A_{om}}{1 + T_m + (2s/\omega_1) + (s^2/\omega_1^2)}$$

Poles are located at $s = -\omega_n(\xi \pm \sqrt{\xi^2 - 1})$, $\xi = \frac{1}{\sqrt{1 + T_m}}$

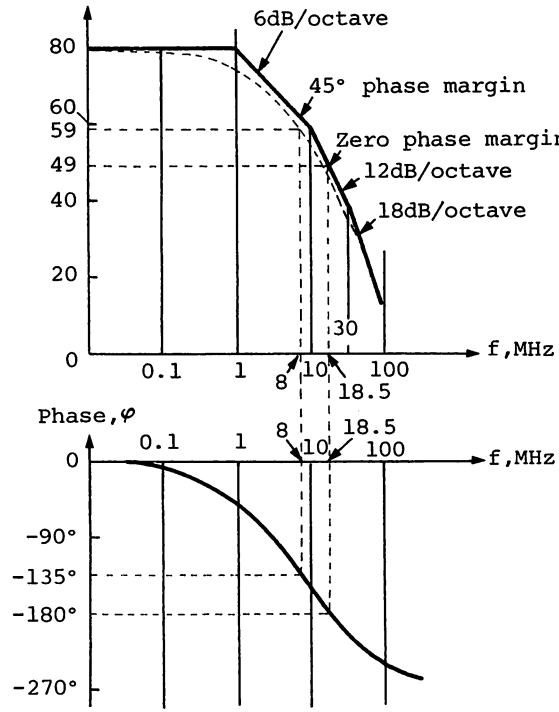
Characteristics:





12.3 STABILIZING NETWORKS

No frequency compensation:



Bode plot for amplifier

The amplifier's open-loop gain is

$$A_o = \frac{-10^4}{\left(1 + \frac{s}{2\pi 10^6}\right)\left(1 + \frac{s}{2\pi \times 10^7}\right)\left(1 + \frac{s}{2\pi \cdot 30 \times 10^6}\right)}$$

If sufficient feedback is applied to make $|T| = 1$ at 18.5 MHZ, the amplifier is said to be marginally stable.

If sufficient feedback is applied to make $|T| = 1$ at a frequency < 18.5MHz, the actual phase at $|T| = 1$ is $< 180°$. The difference between 180° and the actual phase at $|T| = 1$ is called "Phase-Margin".

The frequency at which $|T| = 1$ is called the gain crossover frequency.

$$T(s) = A_o(s) \cdot K/(R_f/R_s), \quad \beta = \frac{K}{(R_f \div R_s)}$$

$$A_v(s) = \frac{A_o(s)}{1 - \beta \cdot A_o(s)} \approx \frac{-1}{\beta} \quad (\text{if } |T(s)| >> 1)$$

For a 45° phase margin,

$$|T(8MHz)| = 1 = \beta\,|A_o(8MHz)| \approx \beta(936), \quad \beta \approx -59dB$$

At low frequencies, $T_m = \beta \cdot A_{om} = 21dB$

For a 45° phase margin:

$$\beta = 1 \,/\, |A_o(\omega \text{ corresponding to } 135°)|$$

$$|T_{max}| = \beta|A_{om}| = A_{om} \div |A_o(\omega \text{ corresponding to } 135°)|$$

Simple lag compensation:

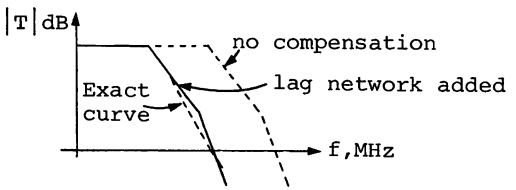
Simple lag compensation is designed to introduce an additional negative real pole in the transfer function of the open-loop amplifier gain, A_o.

$$A_{o1}(s) = A_o(s) \div \left(1 + \frac{s}{\alpha}\right) \ldots.$$

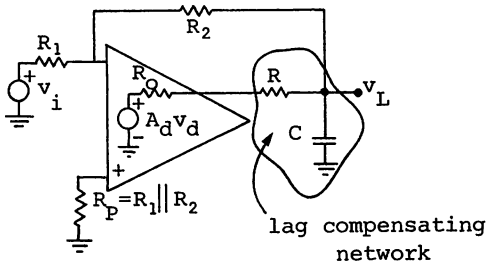
The pole α is adjusted so that $|T|$ drops to OdB at a frequency where the poles of A_o contribute negligible phase shift.

This pole increases T but decreases the cross-over frequency.

Effect of lag compensation:



Lag compensating network:



The break frequency of this lag filter:

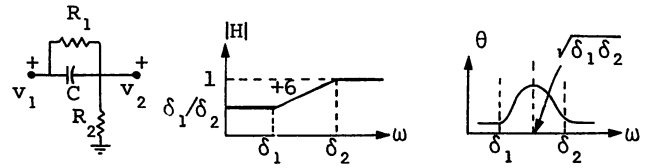
$$\frac{\alpha}{2\pi} \approx \frac{1}{2\pi (R+R_o)C} \quad \ldots \text{ (assuming } R+R_o << R_2).$$

Lead compensation:

The transfer function $H(s) = \frac{s+\delta_1}{s+\delta_2}$

($\delta_2 > \delta_1$, i.e., the pole is located at a higher frequency than the zero.)

Bode diagram for H(s) and the network:



(a) circuit

$\delta_1 = 1/R_1C$

$\delta_2 = \frac{1}{(R_1||R_2)C}$

This network introduces a low-frequency attenuation:

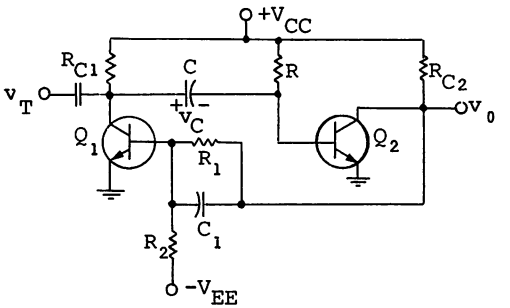
$$H(0) = R_2 \div (R_1+R_2) = \delta_1/\delta_2$$

CHAPTER 13

MULTIVIBRATORS

13.1 COLLECTOR-COUPLED MONOSTABLE MULTIVIBRATORS

Stable-state:



Collector-coupled monostable

In this state Q_1 is off, Q_2 is saturated and v_o is low.

$v_{c_1} \approx V_{cc}$ and $v_{c_2} \approx 0$, the current in R must be sufficient to saturate Q_2, i.e.,

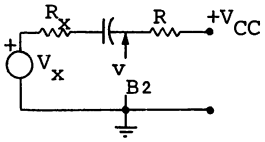
$$I_{B_2} = I_R = \frac{(V_{cc} - V_{BES_2})}{R} >> I_{BS_2} = \frac{I_{cs_2}}{\beta}$$

or

$$\frac{V_{cc} - V_{BES_2}}{R} \geq \frac{V_{cc} - V_{CES_2}}{\beta_2 \cdot R_{c_2}}$$

C_1 is a speed-up capacitor to couple change in v_o to v_{B_1}, turning Q_1 on rapidly.

Circuit operation:



Voltages for the monostable shown in the figure in steady-state and just after triggering into the Quasi-Stable by a trigger pulse at t = 0.

	v_{C_1}	v_{B_2}	v_o	v_{B_1}	Q_1	Q_2
Stable state (t=0)	$\simeq V_{cc}$	$\simeq 0V$	$\simeq 0V$	$< 0V$	off	on
Quasi-stable state ($t=0^+$)	$\simeq 0V$	$\simeq -V_{cc}$	$\simeq V_{cc}$	$\simeq 0V$	on	off

The initial trigger pulse need not be of amplitude V_{cc}. It only starts Q_2 off; the circuit's regenerative action itself drives v_{c_1} to $\approx$ 0v and v_{B_2} to $\approx -V_{cc}$.

Output pulse width:

The equivalent-circuit at the collector of Q_1 at $t = 0^+$ when Q_1 has just turned on and Q_2 has just turned off.

τ (Time constant with which v_{B_2} moves toward V_{cc})

$= (R+R_x) \cdot C \approx R \cdot C$, $(R >> r_{sat})$

$$v_{B_2}(t) = V_F - (V_F - V_I)e^{-t/\tau}$$

(where $V_1 = V_{BE_2} - V_{cc} + V_{CES_1}$

= initial value of v_{B_2}, and

$V_F = V_{cc}$ = the final value of V_{B_2})

T = The duration of the output pulse

$$= \tau \cdot \ln \frac{2V_{cc} - V_{BES_2} - V_{CES_1}}{V_{cc} - V_{BET_2}}$$

For a typical transistor, $V_{BES} + V_{CES} \approx 2V_{BET}$

$$T \simeq \tau \ln 2 \approx 0.69\tau \approx 0.69R_c$$

Recovery time:

This is the time one must wait before the monostable multivibrator should be triggered.

When the quasi-stable state ends at t = T, the output returns low although the circuit has not returned to its stable state.

At $t = T^-$, $v_{c_1} = V_{CES_1}$, $v_{B_2} = V_{BET_2}$ and the voltage across C is

$$v_c = V_{CES_1} - V_{BET_2} \approx 0.$$

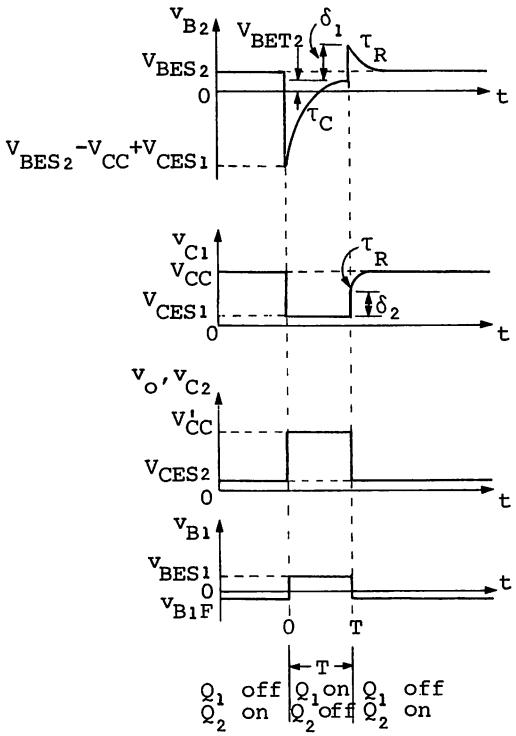
The v_{c_1} increases exponentially from $v_I = V_{CES}$ towards its final value, $V_f = V_{cc}$, with

$$\tau_R \text{ (Recovery time constant)} = (R_{c_1} + (R \| R_{i_2}) \cdot C$$

$$\approx (R_{c_1} + R_{i_2}) \cdot C$$

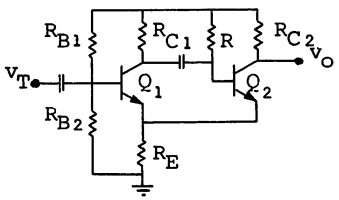
$$V_{cc}' \text{ (the output-volt with } v_{EE} = 0) = \frac{V_{cc} \cdot R_1 + V_{BES_1} \cdot R_{c_2}}{R_1 + R_{c_2}}$$

Waveforms:



Waveforms for the collector-coupled monostable

13.2 EMITTER-COUPLED MONOSTABLE MULTIVIBRATORS



Circuit operation:

$$(R+R_E)I_{B_2} + R_E \cdot I_{c_2} = V_{cc} - V_{BES_2}$$ (KVL equation for Q_2 with Q_1 off and Q_2 on)

$$R_E \cdot I_{B_2} + (R_E+R_{c_2})I_{c_2} = V_{cc} - V_{CE_2}$$

$$v(0) = V_{cc} - R_{c_2}(V_{cc} - V_{CES_2})/(R_{c_2}+R_E)$$

$$= R_E(V_{cc} - V_{CES_2})/(R_{c_2}+R_E) + V_{CES_2}$$

$$v_E(0^-) = v_o(0^-) - V_{CES_2}$$

$$v_{B_2}(\bar{0}) = v_E(0) + V_{BES_2}$$

$$v_{B_1}(\bar{0}) < v_E(\bar{0}) + V_{BET_1}$$ (To maintain Q_1 off)

$$v_{c_1}(\bar{0}) = v_{cc}$$ (with Q_1 off)

$$v_{B_1}(0^+) = V_{B_1} = \frac{V_{cc} \cdot R_{B_2}}{R_{B_1}+R_{B_2}} = v_{B_1}(\bar{0})$$

$$v_E(0^+) = V_{B_1} - V_{BES_1}$$

$$i_{c_1}(0^+) \approx i_{E_1}(0^+) = v_E(\bar{0})/R_E,\ v_{c_1}(0^+) = V_{cc} - i_{c_1}(0^+)R_{c_1}$$

The condition for Q_1 in a quasi-stable state:

$$\frac{R_E + R_{c_1}}{R_E} > \frac{R_{B_1} + R_{B_2}}{R_{B_2}}$$

Voltages with a Narrow Trigger Pulse Applied at t = 0

Parameter	Stable state $t = 0^-$ (Q_1 off, Q_2 saturated)	Quasi-stable state $t = 0+$ (Q_1 saturated, Q_2 off)
v_0	$V_{CC} - (V_{CC} - V_{CES_2}) \frac{R_{C_2}}{R_E + R_{C_2}}$ $\cong V_{CC}\left(1 - \frac{R_{C_2}}{R_E + R_{C_2}}\right)$	V_{CC}
v_E	$v_0(0^-) - V_{CES_2}$ $= (V_{CC} - V_{CES_2})\left(1 - \frac{R_{C_2}}{R_E + R_{C_2}}\right)$ $\cong V_{CC}\left(1 - \frac{R_{C_2}}{R_E + R_{C_2}}\right)$	$V_{B_1} - V_{BES_1}$ $\cong V_{CC} \frac{R_{B_2}}{R_{B_1} + R_{B_2}}$
v_{B_2}	$v_E(0^-) + V_{BES_2}$ $= (V_{CC} - V_{CES_2})\left(1 - \frac{R_{C_2}}{R_E + R_{C_2}}\right)$ $+ V_{BES_2}$ $\cong V_{CC}\left(1 - \frac{R_{C_2}}{R_E + R_{C_2}}\right)$	$v_{B_2}(0^-) + [v_{C_1}(0^+)$ $- v_{C_1}(0^-)]$ $\cong V_{CC}\left(\frac{R_{B_2}}{R_{B_1} + R_{B_2}}\right.$ $\left. - \frac{R_{C_2}}{R_E + R_{C_2}}\right)$
v_{B_1}	$\cong V_{CC} \frac{R_{B_2}}{R_{B_1} + R_{B_2}}$	$\cong V_{CC} \frac{R_{B_2}}{R_{B_1} + R_{B_2}}$
v_{C_1}	V_{CC}	$v_E(0^+) + V_{CES_1}$ $\cong \frac{V_{CC} R_{B_2}}{R_{B_1} + R_{B_2}}$

Condition for operation:

Conditions for Operation of the Monostable

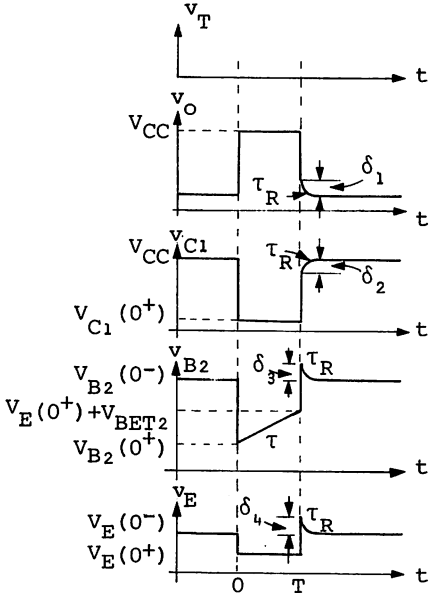
1) $v_{B_1}(0^-) < v_E(0^-) + V_{BET_1}$

2) $i_{B_2}(0^-) > i_{C_2}(0^-)/\beta$

3) $v_{C_1}(0^+) < v_{B_1}(0^+)$

4) $v_{B_2}(0^+) < v_E(0^+) + V_{BET_2}$

Waveforms - With Q_1 saturated and Q_2 off in the quasi-stable state and Q_1 off and Q_2 saturated in the stable state.



Pulse width and recovery:

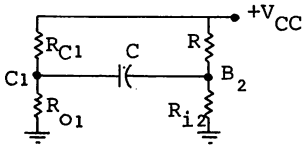
$$T = \tau \cdot \ln \left[\frac{V_F - V_I}{V_F - (V_E(0^+) + V_{BET_2})} \right]$$

$$\approx R \cdot C \ln \left[\frac{1 + \frac{R_{C_2}}{R_E + R_{C_2}} - \frac{R_{B_2}}{R_{B_1} + R_{B_2}}}{1 - \frac{R_{B_2}}{R_{B_1} + R_{B_2}}} \right]$$

$$\tau_R = \text{(Recovery time constant)}$$

$$= (R_{C_1} + \lambda_{\pi_2} + R_E \parallel R_{C_2})C$$

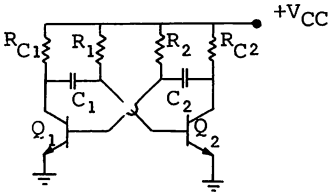
τ_R determines the circuits retrigger rate and the rate of decay of the overshoot.



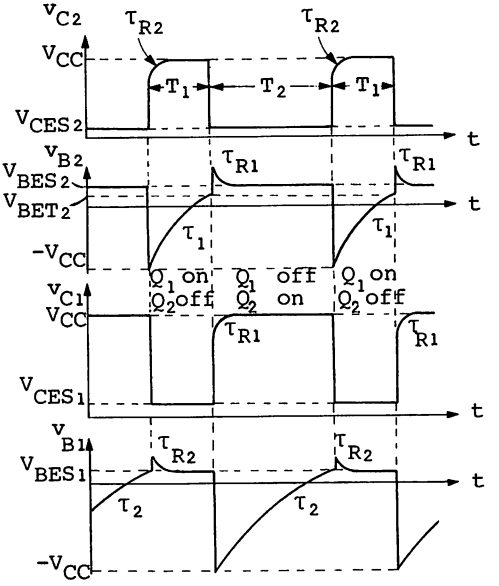
Model of an emitter-coupled monostable multivibrator during the recovery time t > T.

The recovery time for the emitter-coupled monostable multivibrator is greater than in the collector-coupled monostable multivibrator.

13.3 COLLECTOR-COUPLED ASTABLE MULTIVIBRATORS



Typical waveforms at each collector and base:



$$T_1 = 0.69R_1C_1$$

$$T_2 = 0.69R_2C_2$$

$$T_1 \geq 4\tau_{R_2} = 4R_{C_2} \cdot C_2$$

$$T_2 \geq 4\tau_{R_1} = 4R_{C_1} \cdot C_1$$

$$\tau_1 \approx R_1C_1, \quad \tau_2 \approx R_2C_2$$

$$\tau_{R_1} \approx R_{C_1} \cdot C_1, \quad \tau_{R_2} \approx R_{C_2} \cdot C_2$$

13.4 EMITTER-COUPLED ASTABLE MULTIVIBRATORS

When the bias levels in the emitter-coupled monostable multivibrator are properly adjusted, the circuit becomes

astable. Only one capacitor controls the timing of Q_1 and Q_2.

To keep Q_2 active with c open, require

$$\beta \cdot i_{B_2} < i_{CS_2} \text{ or } \beta \cdot \frac{(V_{CC}-V_{B_2})}{R} < \frac{V_{CC}-v_{C_2}}{R_{C_2}},$$

which, with $v_{B_2} = v_{C_2}$, reduces to $\beta \cdot R_{C_2} < R$.

To keep Q_1 active with c open, V_{B_1} should fall inside the following interval:

$$V_{BE} + \frac{R_E(1+\beta)(V_{CC}-V_{BE})}{R+(1+\beta)R_E} < V_{B_1}$$

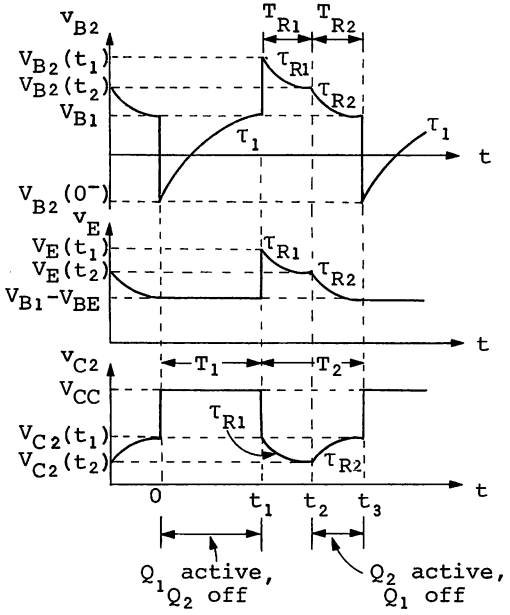
$$< \frac{V_{CC} \cdot R_E[R+(1+\beta)R_{C_1}]+V_{BE} \cdot R \cdot R_{C_1}}{R(R_{C_1}+R_E)+(1+\beta)R_E \cdot R_{C_1}}$$

$$T_1 = RC \ln\left[\frac{V_{CC}-v_{B_2}(0^+)}{V_{CC}-V_{B_1}}\right]$$

$$\tau_{R_1} = (R_{C_1}+R\|R_{C_2}\|R_E)C \approx (R_{C_1}+R_{C_2}\|R_E)C$$

$$\tau_{R_2} = [(1+\beta)R_E\|R]C$$

Waveforms:



Approximate Voltages

	$t = 0^-$ Q_1 off Q_2 active	$t = 0^+$ Q_1 active Q_2 off
v_{C_1}	V_{CC}	$V_{CC} - v_E(0^+)R_{C_1}/R_E$
v_{B_2}	V_{B_1}	$V_{B_1} - v_E(0^+)R_{C_1}/R_E$
v_E	$V_{B_1} - V_{BE_2}$	$V_{B_1} - V_{BE_1}$

CHAPTER 14

LOGIC GATES AND FAMILIES

14.1 LOGIC LEVEL CONCEPTS

"1" and "0" limits must be separated by some voltage range to ensure that the state of a line can be determined even in the presence of noise, etc.

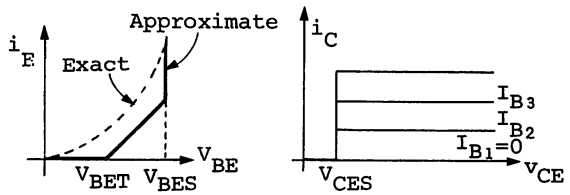
Voltages	G_e V	S_i V
V_{BET}	0.1	0.5
V_{BES}	0.3	0.7
V_{CES}	1.0	0.1
V_{BE} (active)	0.2	0.6

V_{BET}: The v_{BE} threshold voltage below which little conduction occurs.

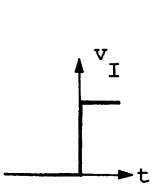
V_{BES} and V_{CES}: The v_{BE} and v_{CE} values in saturation

A high or "1" level corresponding to a voltage above some minimum upper level and a low or "0" to a voltage below some maximum lower level.

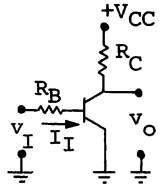
Graphical interpretation of V_{BET}, V_{BES} and V_{CES}:



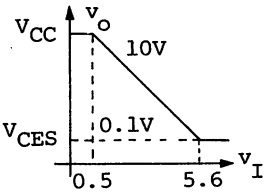
Demonstration of the logic level concept:



Input Waveform



Inverter Circuit



Transfer curve

$I_{CS} = (V_{CC}-V_{CES}) \div R_C$ ....In saturation, with no load

$I_{BS} = I_{CS}/\beta$ ....Corresponding base current of the edge of saturation.

$V_I = [R_B(V_{CC}-V_{CES}) \div (\beta RC)] + V_{BES}$....Voltage to saturate a transistor

The circuit will saturate for any

$$V_I \geq [R_B(V_{CC}-V_{CES}) \div (\beta R_C)] + V_{BES} = 5.65$$

...[Assuming $V_{CC} = +10V$, $R_C = 1K$, $R_B = 10K$]

With v_I satisfying the above equation, $V_o = V_{CES} = 0.1V$.

Inverter logic levels for Fig. 2.2:

v_I,Volts	v_o,Volts
$\geq$ 5.65	0.1
$\leq$ 0.5	10

V	Level
5.65 to 10V	"1"
-2 to 0.5V	"0"

Voltages above 5.65V are designated as "high" or "1" levels; and voltages below 0.5V, as "low" or "0" levels.

The upper "1" limit and the lower "0" limit are arbitrary, depending on power supply and breakdown voltage.

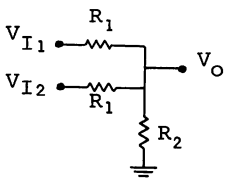
Logic level notation:

Parameter	Definition
V_{OL}	Low or "0" level output voltage
V_{OH}	High or "1" level output voltage
V_{IL}	Low-level input voltage
V_{IH}	High-level input voltage
$\overline{V_{IL}}$	Maximum V_{IL} level
V_{IH}	Minimum V_{IH} level
$\overline{I_{IH}}, I_{IL}$	Input current for $V_I = V_{OH}$ and $V_I = V_{OL}$, respectively.
I_{OH}, I_{OL}	Maximum available output load current for $V_O = V_{OH}$ and $V_O = V_{OL}$, respectively.

14.2 BASIC PASSIVE LOGIC

14.2.1 RESISTOR LOGIC (RL)

AND function can be implemented with passive components only, such as resistors.



V_{I1}(V)	V_{I2}(V)	V_O(V)
0	0	0
0	10	3.3
10	0	3.3
10	10	6.7

$R_1=R_2=1K$

Voltage Truth Table

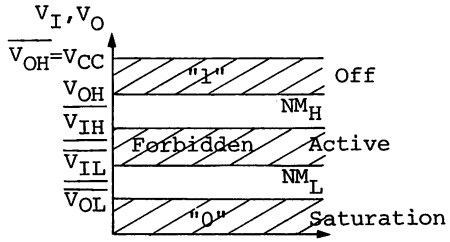
Fan-out (FO):

The number of equivalent gate inputs that can be driven from the output of a similar gate is the fan-out.

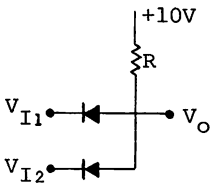
Noise Margin (NM):

This is a measure of the amount of noise that can be tolerated on signal lines before the voltage levels on these lines cease to look like "1s" or "0s".

Graphical Interpretation of NM and "1" and "0":



14.2.2 DIODE LOGIC CIRCUITS



Basic Circuit

V_{I_1} V	V_{I_2} V	V_O V
0	0	0.7
0	5	0.7
5	0	0.7
5	5	5.7

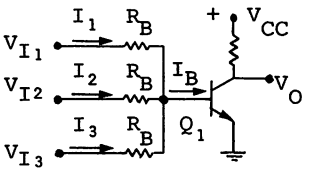
14.2.3 LOGIC CIRCUIT CURRENT, VOLTAGE, AND PARAMETER DEFINITIONS AND NOTATION

Parameter	Definition and test condition
$\underline{V_{IH}}$	Minimum input voltage that will look like a "1" at the input of a gate in worst case.
$\overline{V_{IL}}$	Maximum input voltage that will still look like a "0" at the input of a gate in worst case.
$\underline{V_{OH}}$	Minimum output voltage which, when applied to $FO_H = N_H$ other gate inputs, will look like a "1" at the input of each driven gate with a NM_H.

$\overline{V_{OL}}$	Maximum output voltage which, when applied to $FO_L = N_L$ other gate inputs, will look like a "0" at the input of each driven gate with a NM_L.
I_{IH}	Current required at a gate input with V_{OH} present at the input.
I_{IL}	Current required at a gate input with $\overline{V_{OL}}$ present at the input.
I_{OH}	Available output current when $V_o = V_{OH}$.
I_{OL}	Available output current when $V_o = \overline{V_{OL}}$.
$FO_H = \lvert I_{OH}/I_{IH} \rvert$	Fan-out for a high-level output.
$FO_L = \lvert I_{OL}/I_{IL} \rvert$	Fan-out for a low-level output.
FO	The smaller of FO_H and FO_L.
$NM_H = V_{OH} - V_{IH}$	Noise margin for a high-level output.
$NM_L = \overline{V_{IL}} - \overline{V_{OL}}$	Noise margin for a low-level output.
NM	The smaller of NM_H and NM_L.

14.3 BASIC ACTIVE LOGIC

14.3.1 RESISTOR-TRANSISTOR LOGIC (RTL)



NTL NOR Gate

RTL parameter expressions:

1) $\underline{V_{IH}} = \frac{R_B}{\beta}\left(\frac{V_{CC}-V_{CES}}{R_C} + FO_L|I_{IL}|\right) + 3V_{BES} - 2\overline{V_{OL}}$

2) $\underline{V_{OH}} = NM_H + \underline{V_{IH}}$

3) $\underline{V_{OH}} = (V_{CC}R_B + FO_H V_{BES} R_C)/(R_B + FO_H R_C)$

4) $|I_{OH}| = (V_{CC} - \underline{V_{OH}})/R_C$

5) $I_{IH} = (\underline{V_{OH}} - V_{BES})/R_B$

6) $FO_H = |I_{OH}/I_{IH}|$

7) $\overline{V_{IL}} = V_{BET}$

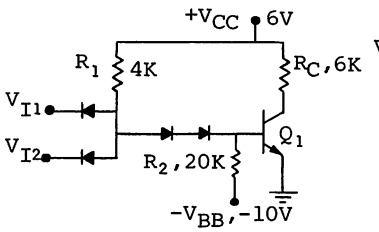
8) $\overline{V_{OL}} = \overline{V_{IL}} - NM_L = V_{CES}$

9) $I_{IL} = (\overline{V_{OL}} - V_{BES})/R_B$

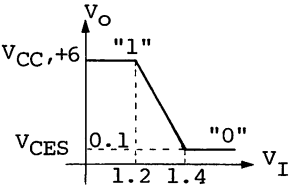
10) $I_{OL} = \beta[\underline{V_{IH}} - V_{BES} - 2(V_{BES} - \overline{V_{OL}})]/R_B - (V_{CC}-V_{CES})/R_C$

11) $FO_L = |I_{OL}/I_{IL}|$

14.3.2 DIODE-TRANSISTOR LOGIC (DTL)



DTL Nand gate



Transfer Characteristics

DTL NAND gate characteristics:

Table 1	Table 2
$\underline{V_{OH}} = 6V$	$FO_L = FO = 9$
$\overline{V_{OL}} = .412V$	$NM_L = NM = .788V$
$\underline{V_{IH}} = 1.4V$	$I_{IL} = -0.83mA$
$\overline{V_{IL}} = 1.2V$	$I_{OL} = 12.2mA$

DTL NAND gate aprameters:

$$\underline{V_{IH}} = V_{DX} + V_{DY} + V_{BES} - V_{D_1}, \quad \overline{V_{IL}} = V_{DX} + V_{DY} + V_{BET} - V_{D_1}$$

$$|I_{IL}| = (V_{CC}-V_D-V_{CES})/R_1 - (V_{CES}+V_D-V_{DX}-V_{DY}+V_{BB})/R_2$$

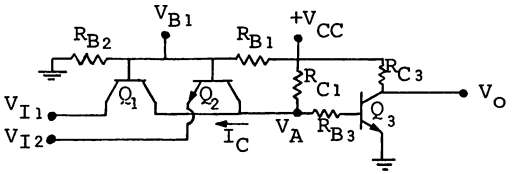
$$I_{OL} = \frac{\beta(V_{CC}-2.1)}{R_1} - \frac{\beta(V_{BES}+V_{BB})}{R_2} - \frac{V_{CC}-V_{CES}}{R_C}$$

$$V_{OL} = V_{CES} + \left[\frac{V_{CC}-V_{OL}}{R_C} + (FO_L)|I_{IL}|\right] r_{sat},$$

$$\overline{V_{OL}} = \overline{V_{IL}} - NM_L$$

14.4 ADVANCED ACTIVE LOGIC GATES

14.4.1 TRANSISTOR-TRANSISTOR LOGIC (TTL)



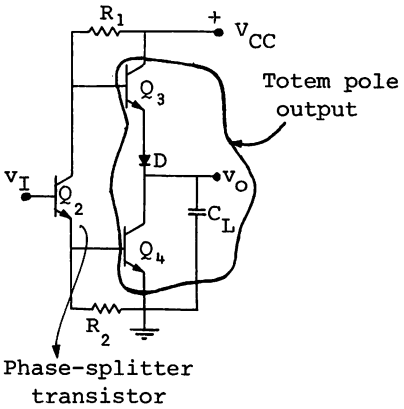
V_{CC}, R_{c_1} and R_{B_3} are chosen so that with Q_1 and Q_2 off, the current from V_{CC} through R_{C_1} is sufficient to saturate Q_3:

$$\frac{V_{CC} - V_{BES_3}}{R_{C_1} + R_{B_3}} = I_{B_3} \geq I_{BS_3}$$

$$= \frac{V_{CC} - V_{CES}}{R_{C_3}} + FO_L I_{IL}$$

Q_1 and Q_2 are off when both inputs V_{I_1}, and V_{I_2}, are low. Furthermore, Q_3 will be turned of if Q_1 or Q_2, or both are turned on when V_{I_1} or V_{I_2}, or both, are high. Hence, this circuit acts as a NAND gate.

Totem-pole output with phase-splitter driver:

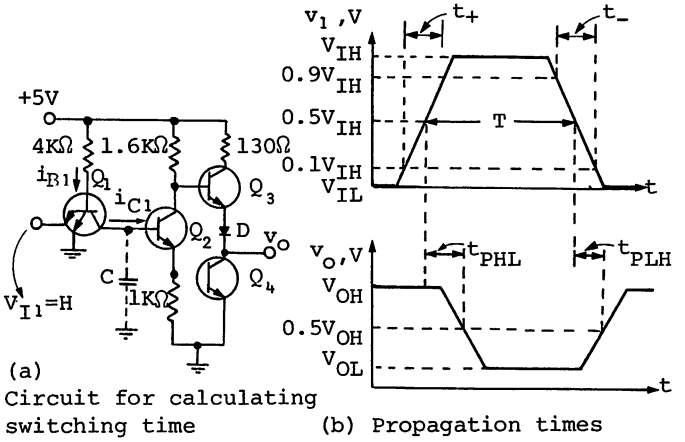


The circuit's response to a positive pulse at the base of Q_2: With v_I low, Q_2 is off, V_{C_2} is high and Q_3 is on, while Q_4 is off and v_o is high.

When v_I goes positive, Q_2 saturates and V_{C_2} droops, turning Q_3 off. V_{E_2} then rises and Q_4 saturates. $(\beta+1)I_{B_4}$ output current quickly discharges C_L and v_o rapidly falls to V_{CES}. When v_I drops from a high level to

OV, Q_2 turns off. V_{E_2} falls to OV, turning Q_4 off; and V_{C_2} rises, turning on Q_3. Q_3 operates as an EF and quickly charges C_L with the large available current $(\beta+1)I_{B_3}$ and v_o rapidly rises.

The totem-pole output thus utilizes EF Q_3 to rapidly raise v_o and the CE transistor Q_4 to rapidly discharge v_o. The phase splitter Q_2 provides the proper phase drive for the totem-pole output transistors. Other topologies, such as DTL, can also use this output connection.

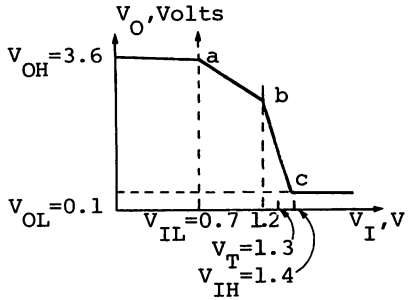


SWITCHING AND PROPAGATION TIMES

Characteristics:

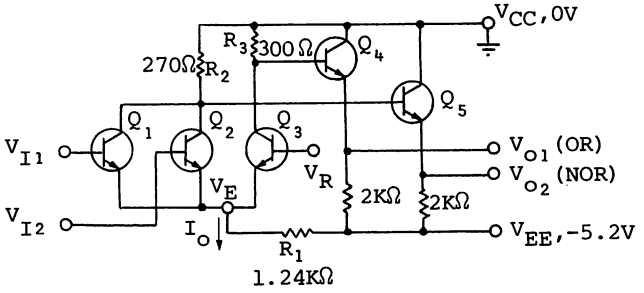
Guaranteed Input and Output Voltage Levels for TTL

Parameter	Value, V	Interpretation for a TTL NAND gate
$\overline{V_{IL}}$	0.8	An input voltage $\leq$ 0.8V is guaranteed to turn on Q_1(E-B junction forward biased).
$\underline{V_{IH}}$	2.0	An input voltage $\geq$ 2.0V is guaranteed to turn off Q_1(E-B junction reverse biased).
$\overline{V_{OL}}$	0.4	With $V_I \leq \overline{V_{IL}}$, the output is guaranteed to be $\leq$ 0.4V under full fan-out.
$\underline{V_{OH}}$	2.4	With $V_I \geq \underline{V_{IH}}$, the output is guaranteed to be $\geq$ 2.4V under full fan-out.



TTL Transfer curve

14.4.2 EMITTER-COUPLED LOGIC (ECL)



Basic ECL OR/NOR gate

CHAPTER 15

BOOLEAN ALGEBRA

15.1 LOGIC FUNCTIONS

15.1.1 NOT FUNCTION

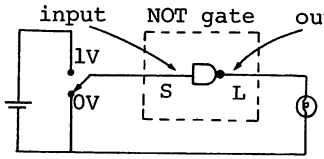


Fig. (a) Circuit

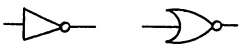


Fig. (b) Symbols

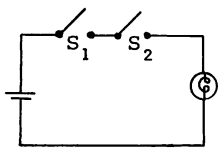
Logic equation and truth table:

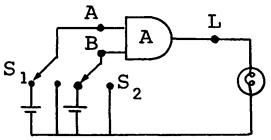
$L = \overline{S}$

S	$L=\overline{S}$
1	0
0	1

15.1.2 AND FUNCTION

The AND functioning circuit:



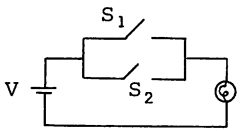


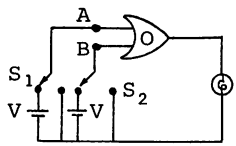
Logic equation and truth table:

L = A * B

A	B	L
0	0	0
0	1	0
1	0	0
1	1	1

15.1.3 OR FUNCTION





Logic equation and truth table:

L = A + B

A	B	L
0	0	0
0	1	1
1	0	1
1	1	1

15.2 BOOLEAN ALGEBRA

Boolean Theorems:

Theorem	Name
A + B = B + A A • B = B A	Commutative law
(A+B)+C = A+(B+C) (A•B)•C = A•(B•C)	Associative law

$A \cdot (B+C) = A \cdot B + A \cdot C$ Distributive law
$A + (B \cdot C) = (A+B) \cdot (A+C)$

$A + A = A$ Identity law
$A \cdot A = A$

$\overline{\overline{A}} = \overline{\overline{A}}$ Negation
$\overline{\overline{A}} = A$

$A + A \cdot B = A$ Redundancy
$A \cdot (A+B) = A$

$0 + A = A$
$1 \cdot A = A$
$1 + A = 1$
$0 \cdot A = 0$

$\overline{A} + A = 1$
$\overline{A} \cdot A = 0$

$A + \overline{A} \cdot B = A + B$
$A \cdot (\overline{A} + \overline{B}) = A \cdot \overline{B}$

$\overline{A+B} = \overline{A} \cdot \overline{B}$ De Morgan's laws
$\overline{A \cdot B} = \overline{A} + \overline{B}$

Proof of theorems:

Proof of theorem $(A+B) \cdot (A+C) = A + (B \cdot C)$

$$(A+B) \cdot (A+C) = AA + AB + AC + BC$$
$$= A + A(B+C) + BC$$
$$= A(1+B+C) + BC$$
$$= A + BC$$

Proof of theorem $A + A \cdot B = A$

A	B	A • B	A+A • B
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

Proof of theorem $A + \overline{A} \cdot B = A + B$

A	B	A+B	$\overline{A}$	$\overline{A}B$	$A+\overline{A}B$
0	0	0	1	0	0
0	1	1	1	1	1
1	0	1	0	0	1
1	1	1	0	0	1

Proof of theorem $\overline{A+B} = \overline{A} \cdot \overline{B}$

A	B	A+B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Manipulations of logic equations:

Simplify $L = \overline{X}Y + XY + \overline{X}\,\overline{Y}$

$= Y(X+\overline{X}) + \overline{X}\,\overline{Y}$

$= Y(1) + \overline{X}\,\overline{Y} = Y + \overline{X}\,\overline{Y}$

$= Y + \overline{X}$

If $L = \overline{X}Y + X\overline{Y}$, find $\overline{L}$.

$\overline{L} = \overline{\overline{X}Y + X\overline{Y}}$

$= (\overline{\overline{X}Y})\,(\overline{X\overline{Y}})$

$= (\overline{\overline{X}}+\overline{Y})(\overline{\overline{X}}+\overline{\overline{Y}})$

$= (X+\overline{Y})(\overline{\overline{X}}+Y)$

$= X\overline{X} + XY + \overline{Y}\,\overline{X} + \overline{Y}Y$

$= XY + \overline{Y}\,\overline{X}$

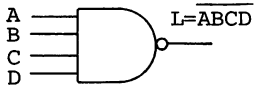
15.3 THE NAND AND NOR FUNCTIONS

The NAND function:

Logic equation: $L = \overline{ABCD...}$

The NAND operation is commutative, i.e., $L = \overline{ABC} = \overline{BAC} = ...$, but not associative.

Truth table:



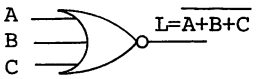
A	B	L	A·B
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

The NOR function:

The logic equation is $L = \overline{A+B}$

The NOR operation is commutative, i.e., $L = \overline{A+B+C...} = \overline{B+A+C...}$ but it is not associative.

Truth table:



A	B	L	A+B
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

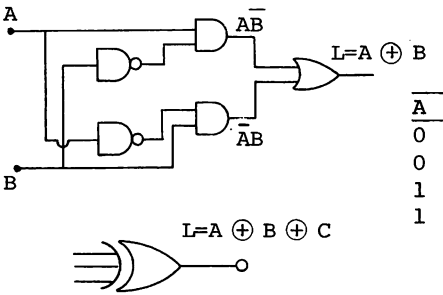
The exclusive OR function:

The logic equation is $L = A \oplus B = \overline{A}B + A\overline{B}$

The function is both commutative and associative.

In practice, these gates with more than two inputs are not available.

Truth table:



A	B	Output L
0	1	0
0	1	1
1	0	1
1	1	0

15.4 STANDARD FORMS FOR LOGIC FUNCTIONS

Sum of products (SP):

The logic function is written as a simple sum of terms, e.g.,

$$L = (\bar{W} + XY)(X + YZ)$$

$$= (\bar{W} + XY)X + (\bar{W} + XY)YZ$$

$$= \bar{W}X + XXY + \bar{W}YZ + XYYZ$$

$$= \bar{W}X + XY + \bar{W}YZ + XYZ \text{ (the desired form).}$$

To find the logic equation for L from the truth table:

Select the rows for which L = 1, these are called "Minterms."

Find the logic expression for these in the product form.

i.e., Row #3 (Minterm): $\bar{X}Y\bar{Z} = \bar{0}\ 1\ \bar{0} = 1$

Take the sum of all the minterms:

$$L = \overline{X}Y\overline{Z} + \overline{X}YZ + X\overline{Y}\overline{Z} + XY\overline{Z} + XYZ$$

Row #	X	Y	Z	L
1	0	0	0	0
2	0	0	1	0
3	0	1	0	1
4	0	1	1	1
5	1	0	0	1
6	1	0	1	0
7	1	1	0	1
8	1	1	1	1

Product of sums (PS):

This consists of a product of terms in which each term consist of a sum of all or part of the variables.

$$L = (\overline{W}+XY)(X+YZ) = (\overline{W}+X)(\overline{W}+Y)(X+Y)(X+Z)$$

To find a PS form from the truth table:

Pick-up rows for which L = 0, these are called the "Maxterms".

Express the logic expression for these in the sum form, i.e.,

For row #1: $X + Y + Z$

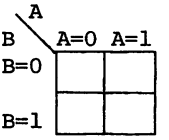
Take product of all these "Maxterms", i.e.,

$$L = (X+Y+Z)(X+Y+\overline{Z})(\overline{X}+Y+\overline{Z})$$

15.5 THE KARNAUGH MAP

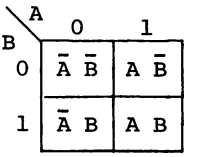
It is a graphical technique for reducing logic equations to a minimal form.

Two variable Karnaugh map:



Two-variable map

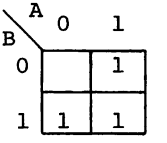
A	B	Term in logic equation = to 1
0	0	$\bar{A}\,\bar{B}$
0	1	$\bar{A}\,B$
1	0	$A\,\bar{B}$
1	1	$A\,B$



Correspondence with truth-table

Truth Table

A	B	L
0	0	0
0	1	1
1	0	1
1	1	1



K map for $L=\bar{A}B+A\bar{B}+AB$

An example

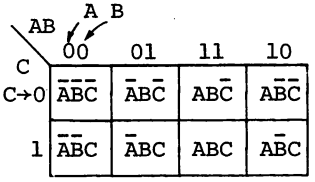
Set of rules for simplification:

A group of two adjacent cells combines to yield a single variable.

A single cell which can't be combined represents a two-variable term.

It is permissible for groups to overlap because of the fact that in boolean algebra, A+A = A.

Three-variables map:



A primary map

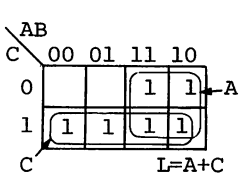
The set of rules for simplification:

A group of 4 adjacent cells (in-line or square) combines to yield a single variable.

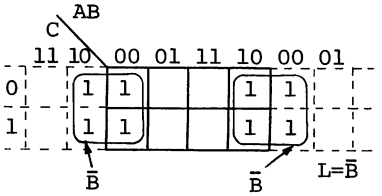
A group of two adjacent cells combines to yield a two-variable term.

A single cell which can't be combined represents a 3-variable term.

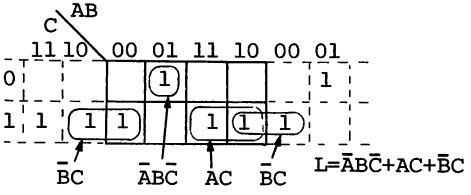
Use of these terms:



Four-cell grouping



Map continuity

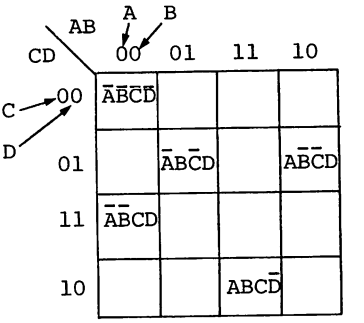


Two-cell groupings and single cell.

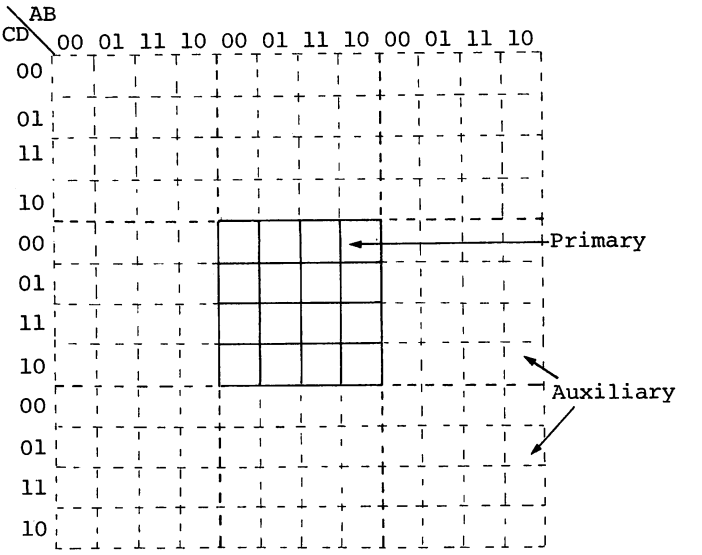
Four-variable map:

The rules are:

Eight adjacent cells yield a single variable. 4-adjacent cells yield a two-variable term. Two adjacent cells yield a 3-variable term. Individual cells represent 4-variable terms.



Primary map



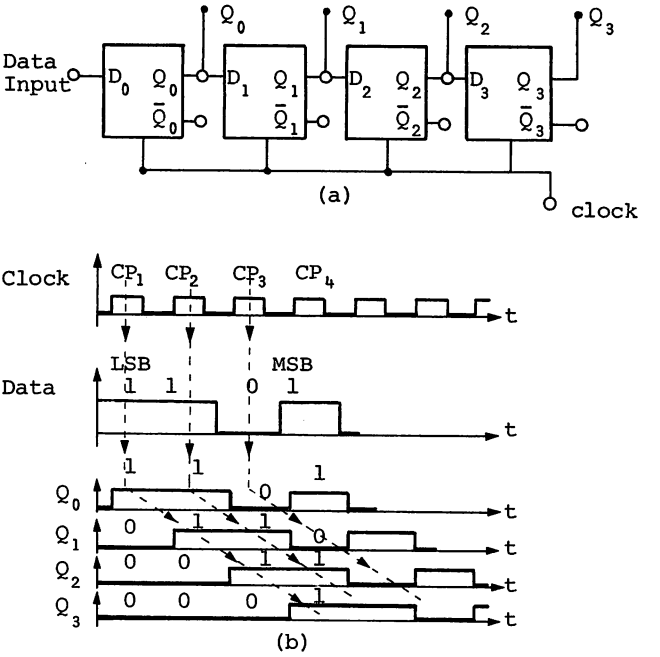
Continuity with auxiliary maps

CHAPTER 16

REGISTORS, COUNTERS AND ARITHMETIC UNITS

16.1 SHIFT REGISTERS

16.1.1 SERIAL-IN SHIFT REGISTERS



Four-bit shift registers: (a) logic diagram; (b) waveforms

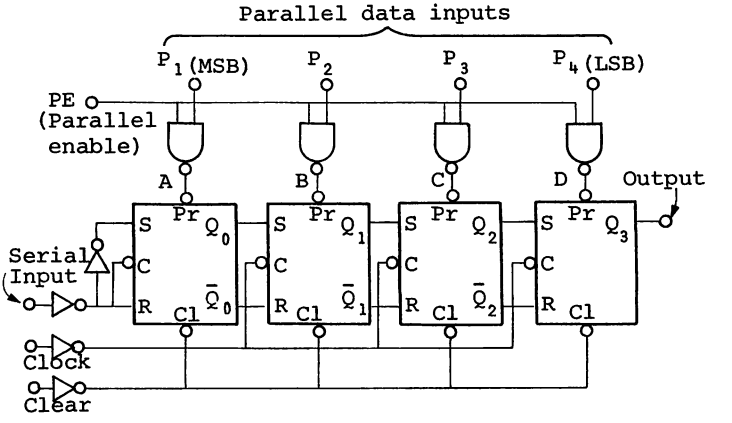
Data can be taken from this register in either serial or parallel form. For serial removal, it is necessary to apply four additional clock pulses; the data will then appear on Q_3 in serial form.

To read data in parallel form, it is only necessary to enter the data serially. Once the data are stored, each bit appears on a separate output line, Q_0 to Q_3.

16.1.2 PARALLEL-IN SHIFT REGISTERS

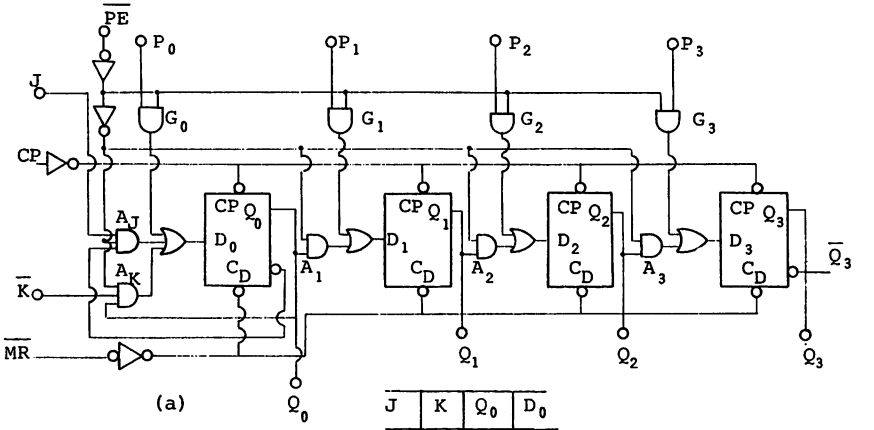
The flip-flops have asynchronous preset and clear capability.

The unit has synchronous serial or asynchronous parallel-load capability and a clocked serial output.



Simplified 54/7494 4-bit shift register.

16.1.3 UNIVERSAL SHIFT REGISTERS



J	K	Q_0	D_0
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b)

$\overline{PE}$=parallel enable

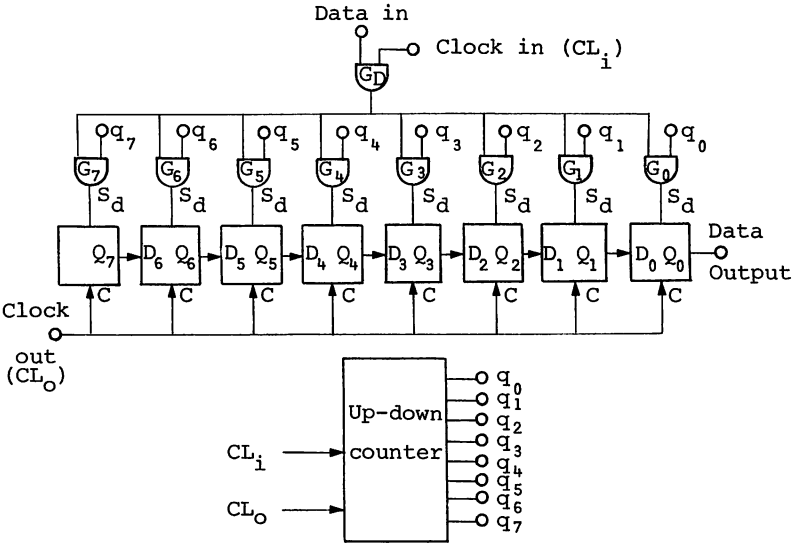
$P_0,\ldots,P_3$=parallel inputs

$\overline{MR}$=master reset

$J,\overline{K}$=inputs

$Q_0,\ldots,Q_3$=outputs

This register contains four clocked master-slave flip-flops with D inputs.



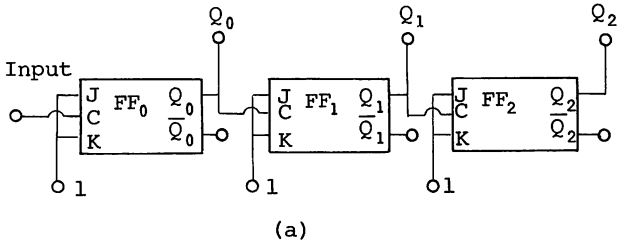
16.2 COUNTERS

16.2.1 THE RIPPLE COUNTER

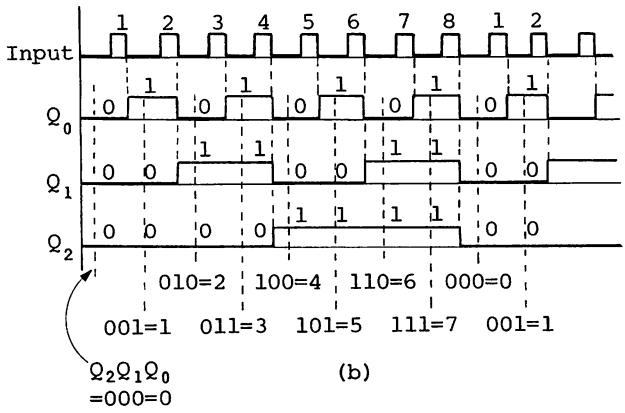
This counter uses the maximum count capability of the three stages; hence, it is a mod-8 counter (the maximum modulus of an N-flipflop counter is 2^N).

Count C = $(Q_2 \times 2^2) + (Q_1 \times 2^1) + (Q_o \times 2^o)$

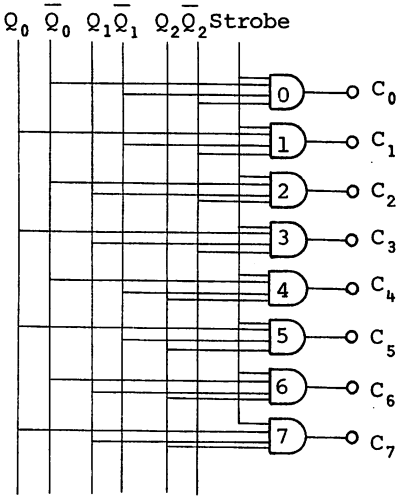
To obtain the decimal output, a binary-to-decimal decoder as shown below is used.



(a)

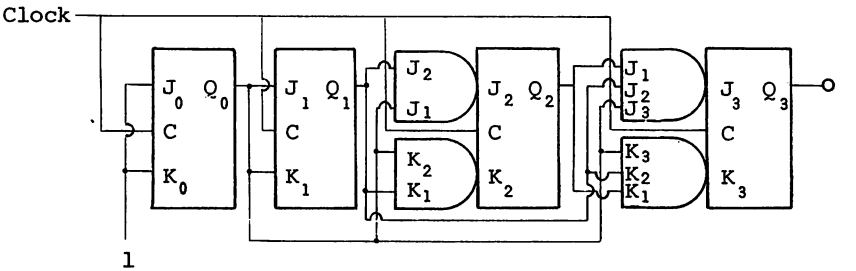


Mod-8 ripple counter: (a) logic diagram;
(b) waveforms.



Binary-to-decimal decoder

16.2.2 THE SYNCHRONOUS COUNTER



Circuit of synchronous parallel counter

The state table:

State table		
Counter state	Q_1 (2^1)	Q_0 (2^0)
0	0	0
1	0	1
2	1	0
0	0	0
1	0	1
2	1	0
0	0	0
⋮	⋮	⋮

FF_0 must change state (toggle) with each clock pulse. This is done by connecting J_0 and K_0 to a high level.

FF_1 must change state whenever $Q_0 = 1$. This is achieved by connecting J_1 and K_1 directly to Q_0.

FF_2 changes state only when $Q_0 = Q_1 = 1$. Thus Q_0 and Q_1 are connected through AND gates to J_2 and K_2.

FF_3 changes state only when $Q_0 = Q_1 = Q_2 = 1$. This requires 3-input AND gates connecting Q_0, Q_1 and Q_2 to J_3 and K_3.

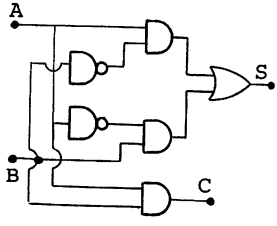
Each following stage requires an additional input to the AND gate.

The propagation delay of an F-F increases with the load and limits the speed attainable with the counter.

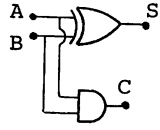
$$f_{max} \leq \frac{1}{t_{pd}(FF_3) + t_{pd}(AND) + t_s}$$

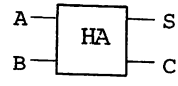
16.3 ARITHMETIC CIRCUITS

16.3.1 ADDITION OF TWO BINARY DIGITS, THE HALF ADDER



Circuit with AND, OR, & NOT gates





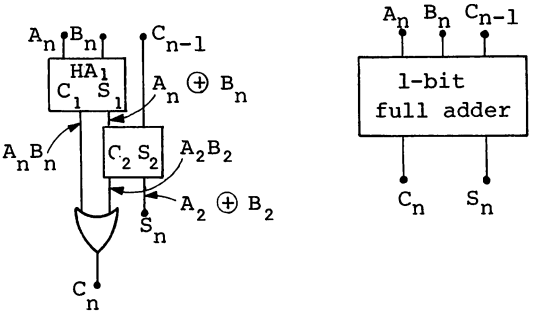
Truth Table:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The logic equations:

$$C = AB \text{ and } S = \overline{A}B + A\overline{B}$$

16.3.2 THE FULL ADDER



Truth table for adding A_n and B_n and a carry C_{n-1}.

A_n	B_n	C_{n-1}	S_n	C_n
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

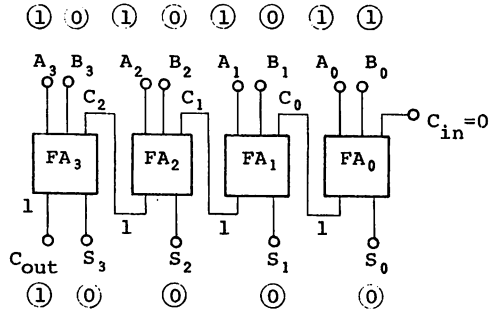
Logic equations:

$$S_n = C_{n-1}(\overline{A}_n\overline{B}_n + A_nB_n) + \overline{C}_{n-1}(\overline{A}_nB_n + A_n\overline{B}_n)$$

$$= C_{n-1} \oplus (A_n \oplus B_n)$$

$$C_n = A_nB_n + C_{n-1}(A_n + B_n)$$

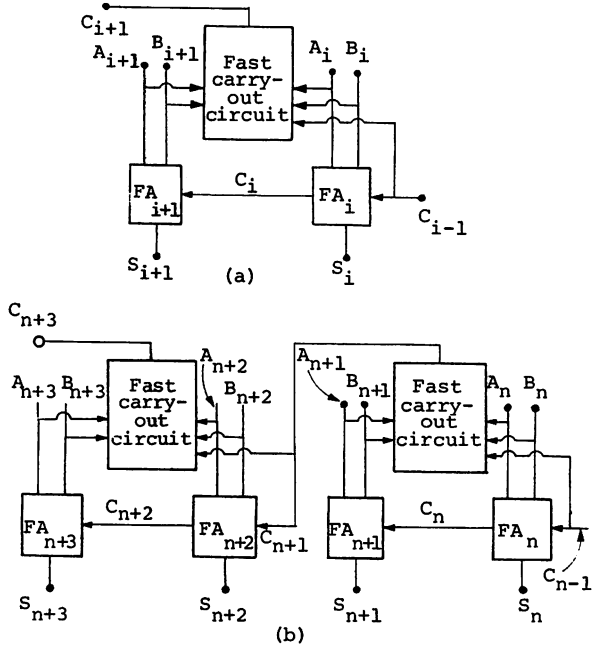
16.3.3 PARALLEL ADDITION



4-bit parallel adder.

If the propagation delay time $t_A = 2t_{pd}$ is the same for each adder, then the carry from FA_0 appears at FA_1 after time t_A, the carry from FA_1 appears at FA_2 after $2t_A$, and so on.

16.3.4 LOOK-AHEAD-CARRY ADDERS



Carry-circuits: (a) 2-bit adder with a fast carry output; (b) 4-bit adder with fast carry output.

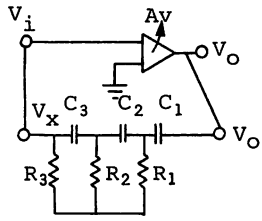
CHAPTER 17

OSCILLATORS

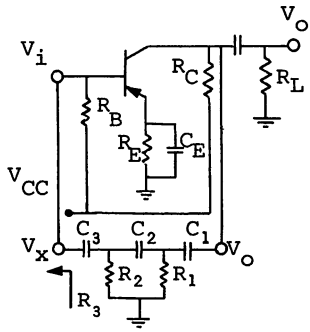
17.1 HARMONIC OSCILLATORS

A harmonic oscillator generates a sinusoidal output.

17.1.1 THE RC PHASE SHIFT OSCILLATOR



Amplifier with RC feedback network



CE version of the circuit

For the feedback network:

$$R_3C_3 = R_2C_2 = R_1C_1 = RC$$

$$\frac{V_i}{V_o} = \frac{j\omega RC}{1+j\omega RC}$$

The overall transfer function $= \frac{V_x}{V_o} = \left(\frac{j\omega RC}{1+j\omega RC}\right)^3$

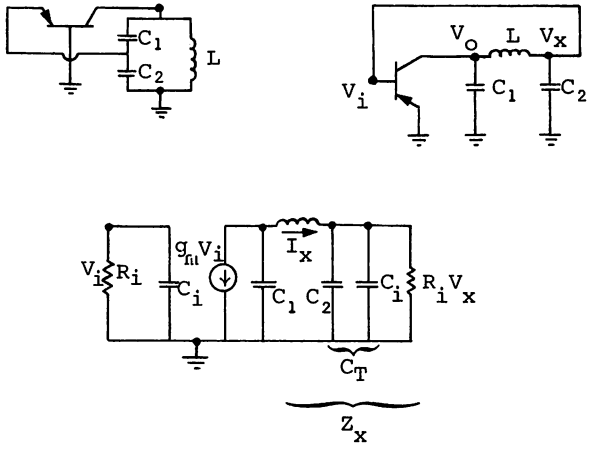
The circuit will oscillate at the frequency for which the phase shift from V_o to V_x is 180°.

$$f_o = 0.577/2\pi RC$$

$$\left| \frac{V_x}{V_o} \right| = \left(\frac{0.577}{1.58} \right)^3 = \frac{1}{8},$$

i.e., the voltage is attenuated by a factor of 8.

17.1.2 THE COLPITTS OSCILLATOR



$$V_x = I_x \cdot Z_x, \quad I_x = -g_m \cdot V_i \cdot \frac{1/j\omega C_1}{(1/j\omega C_1)+j\omega L+Z_x}$$

$$V_x = V_i \text{ and } I_x - Z_x = \frac{I_x \left[1/j\omega C_1+j\omega L+Z_x\right]}{-g_m\left[1/j\omega C_1\right]}$$

$$Z_x = \frac{R_i\left[1/j\omega C_T\right]}{R_i+(1/j\omega C_T)}$$

$$1 + g_m R_i - \omega^2 LC_1 + j(\omega c_1 R_i + \omega C_T R_i - \omega^3 LC_1 C_T R_i) = 0$$

$$\omega^3 LC_1C_T \cdot R_i = \omega C_1R_i + \omega C_T \cdot R_i, \quad \omega^2 = \frac{C_1 + C_T}{L \cdot C_T \cdot C_1}$$

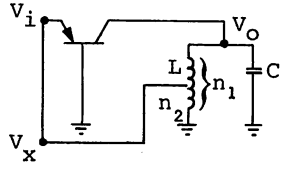
$$f_o = 1/2\sqrt{LC}, \quad \text{where } C = \frac{C_1 \cdot C_T}{C_1 + C_T}$$

Condition for sustained oscillations:

$$g_m R_i = C_1/C_T \quad (\text{since } R_i \approx r_{b'e},\ g_m R_i \approx g_m r_{b'e} = h_{fe}),$$

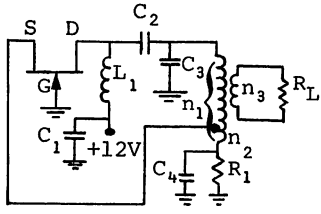
$$h_{fe} = C_1/C_T$$

17.1.3 THE HARTLEY OSCILLATOR

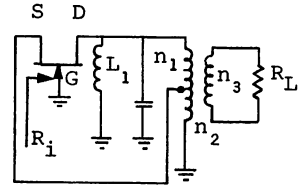


The feedback factor: $\beta_v = \frac{V_x}{V_o} = \frac{h_2}{h_1}$

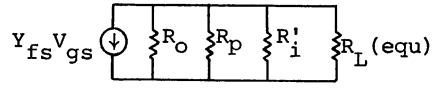
The Hartley oscillator and its ac and output equivalent circuit:



(a) Circuit



(b) Equivalent A.C. circuit



(c) Output equivalent circuit

The voltage amplification: $A_v \approx R'_L \gamma_{fs}$

The Barkhausen's criterion: $\frac{n_2 \cdot R'_L}{n_1} \gamma_{fs} = 1\angle 0°$

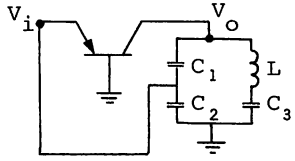
$$\frac{n_2}{n_1} = \frac{1}{R'_L \gamma_{fs}}$$

17.1.4 THE CLAPP OSCILLATOR

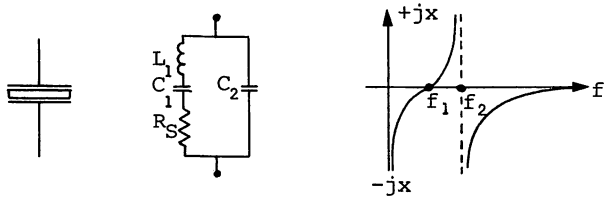
$$\left| j\omega_o L - \frac{j}{\omega_o C_3} \right| = \left| \frac{-j}{\omega_o C} \right|$$

$$\omega_o L - \frac{1}{\omega_o C_3} = 1/\omega_o C$$

$$f_o = 1/2\pi \sqrt{L \frac{C_3 C}{C_3 + C}}$$



17.1.5 THE CRYSTAL OSCILLATOR



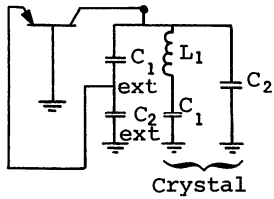
Resonant crystal, equivalent circuit and impedance characteristics

The series resonant frequency:

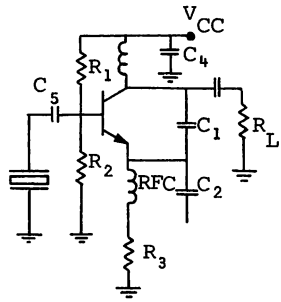
$$f_1 = \frac{1}{2\pi\sqrt{L_1 C_1}}, \quad f_2 = \text{The parallel resonant}$$

$$\text{frequency} = \frac{1}{2\pi\sqrt{L_1 C_1 C_2/(C_1+C_2)}} = f_1\sqrt{1+\frac{C_1}{C_2}}$$

The Clapp and Colpitts crystal oscillators:



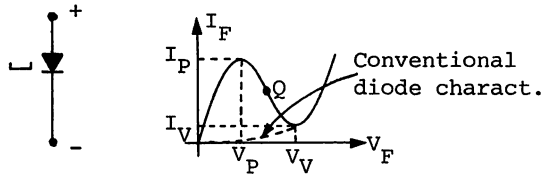
Clapp crystal Oscillator



Colpitts Oscillator

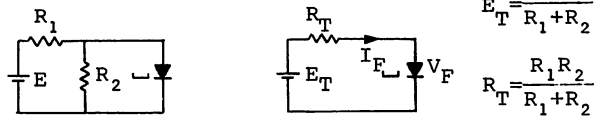
17.1.6 TUNNEL DIODE OSCILLATORS

These oscillators exhibit negative resistance when suitably biased.



Dynamic resistance: $r = \Delta V_F / \Delta I_F$.

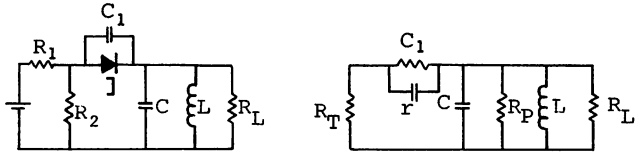
Tunnel diode dc biasing circuit:



$$E_T = \frac{ER_2}{R_1+R_2}$$

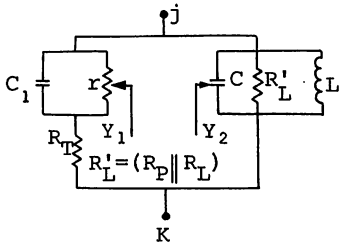
$$R_T = \frac{R_1 R_2}{R_1+R_2}$$

Tunnel diode oscillator:



Oscillator Equivalent circuit

AC equivalent circuit for deriving criteria for oscillations:



$$Y_{jk} = Y_1 + Y_2, \quad Y_1 = 1/Z_1$$

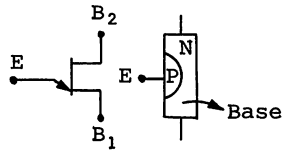
$$Z_1 = R_T + \left(r \parallel \frac{1}{j\omega c_1} \right)$$

$$R_T = \frac{-r}{1+\omega^2 r^2 C_1^2} \quad \text{(The condition for oscillations at } \omega \text{)}$$

$$f_{max}^2 = \frac{-(r+R_T)}{r^2 R_T C_1^2 (2\pi)^2} = \text{The highest possible frequency.}$$

$$f_o \text{ (The actual frequency of oscillations)} = \frac{1}{2\pi\sqrt{LC}} \cdot \frac{1}{\sqrt{1 + \frac{r \cdot C_1}{C(r+R_T)}}}$$

17.2 RELAXATION OSCILLATORS



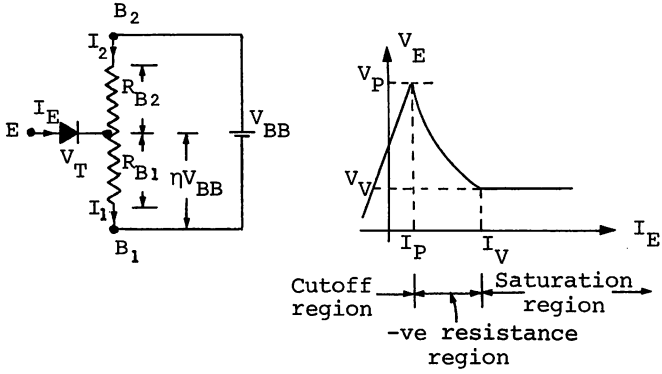
The unijunction transistor (UJT) oscillator:

Useful relationships:

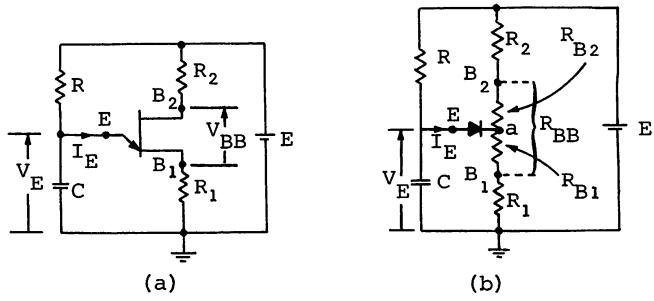
$R_{BB} = R_{B1} + R_{B2}$ (R_{BB} is the interbase resistance)

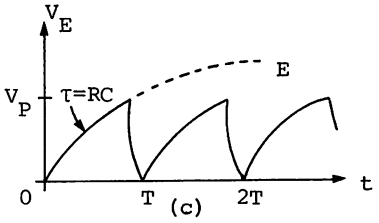
n = The standoff ratio = $R_{B1}/R_{B1} + R_{B2}$

Equivalent circuit and characteristics:



UJT oscillator:





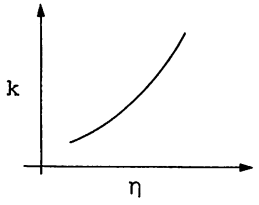
(a) Circuit of UJT oscillator; (b) AC equivalent circuit for (a); (c) emitter voltage waveform for the circuit of (a).

$$T = (R \cdot C)\ln\left|\frac{1}{1-n}\right|, \quad K = \ln\left|\frac{1}{1-n}\right|$$

f_o = The frequency of oscillations

= 1/RCK

Plot of K as a function of n:

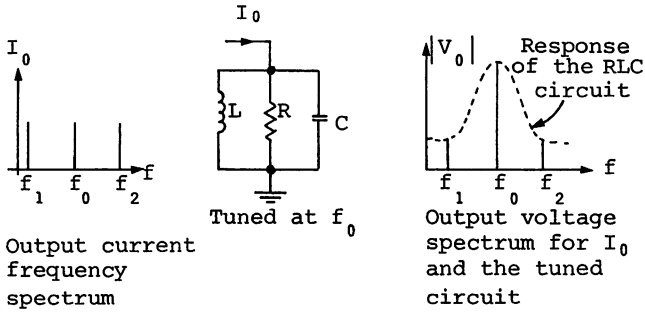


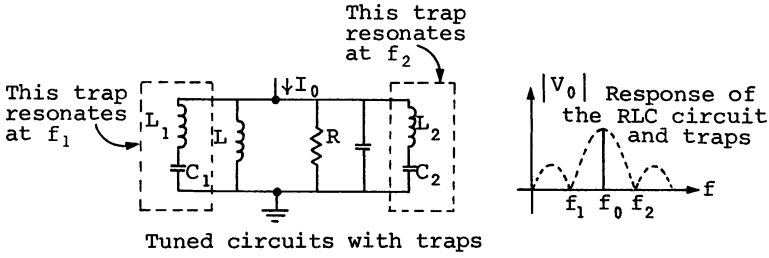
CHAPTER 18

RADIO-FREQUENCY CIRCUITS

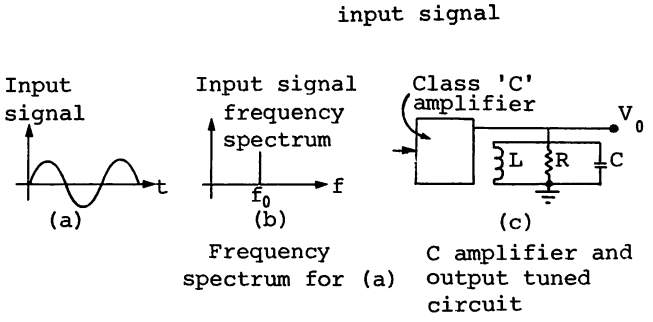
18.1 NON-LINEAR CIRCUITS

A non-linear circuit is defined as any circuit that produces frequencies not present in the input signal.

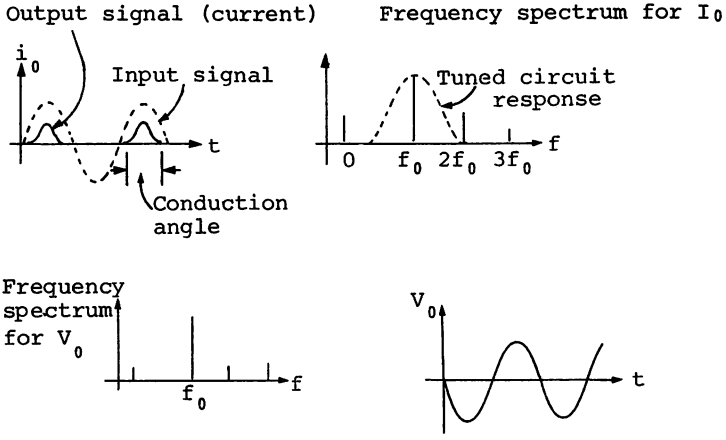




Class 'C' amplification:

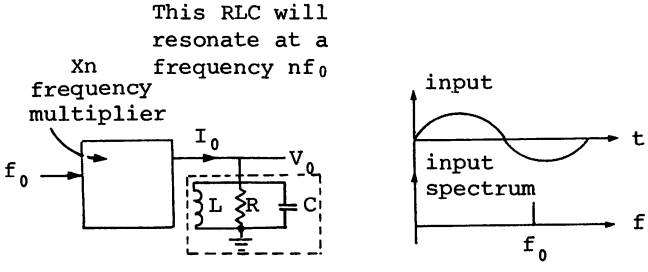


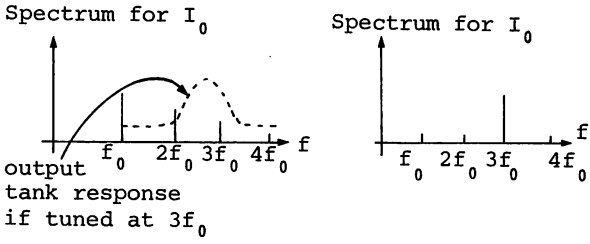
Waveforms and frequency spectra for a class 'C' circuit:

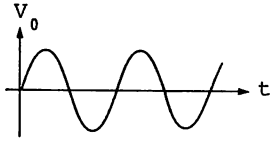


Frequency multiplication:

Diagram and signals for a frequency multiplier:

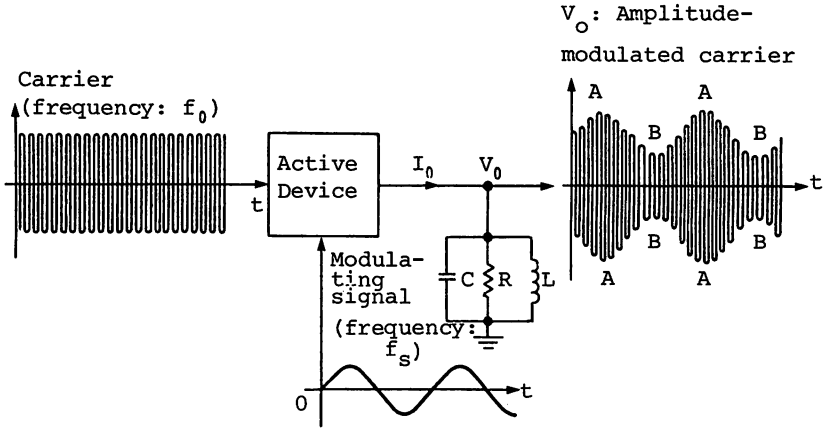




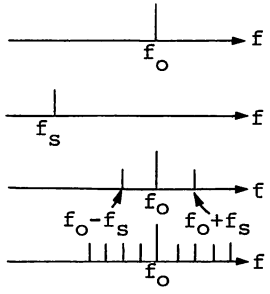


Mixing

Two signals are combined to yield an output signal with a frequency content which includes both the sum and difference of the two input frequencies.



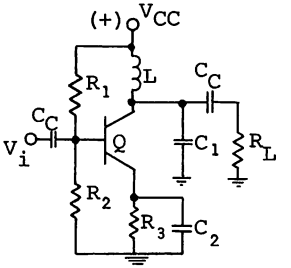
Block diagram of amplitude modulation system



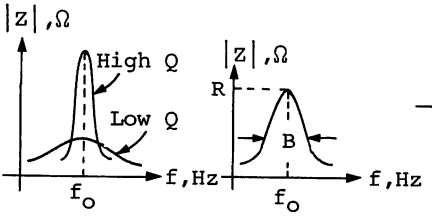
18.2 SMALL-SIGNAL RF AMPLIFIERS

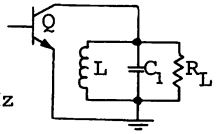
Tuned amplifiers are mainly characterized by 1) center frequency f_o; 2) a bandwidth (B of 3dB 3) power gain at f_o: G_o and a noise figure at f_o, NF.

Basic circuits:



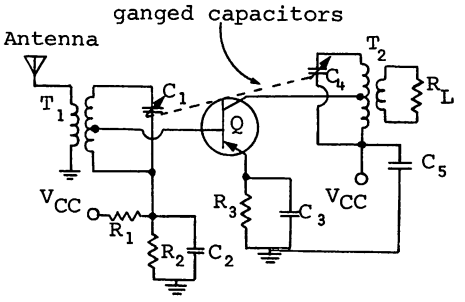
(a)

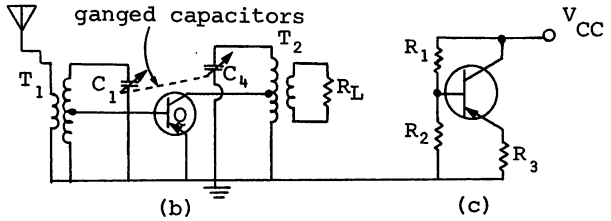




Equi. load seen by the transistor

Bandwidth is a function of the circuit Q. A high Q means a narrow bandwidth, while a lower Q results in a wider bandwidth.

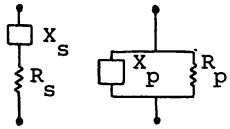




(a) RF amplifier with tuned input and output;
(b) AC circuit for (a); (c) DC circuit for (a)

Both the transformers are wound around an air core, that is, a non-magnetic core. The air core is used at high frequencies because the inductance required is small and the core losses are small, yielding a high Q.

18.3 TUNED CIRCUITS



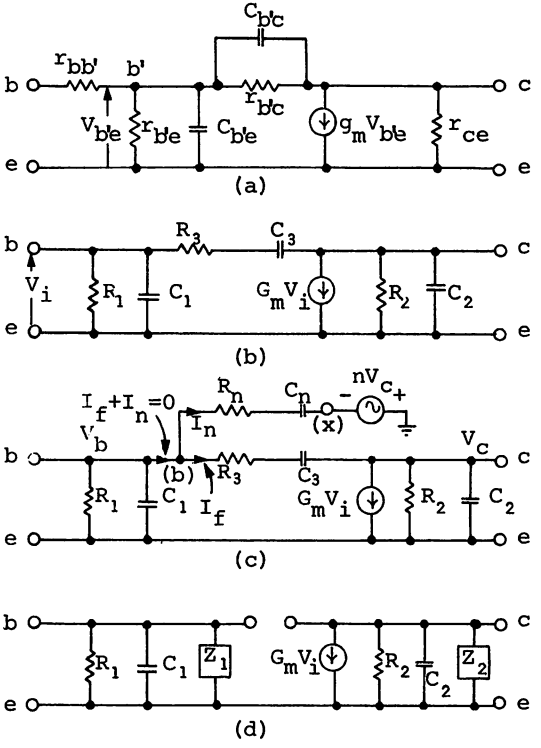
$$Q = \frac{X_s}{R_s}, \quad Z_s = R_s \pm jX_s, \quad Z_p = (R_p)(\pm jX_p)/R_p \pm jX_p.$$

$$Z_s = Z_p \rightarrow R_s = \frac{R_p X_p^2}{R_p^2 + X_p^2}, \quad X_s = \frac{X_p R_p^2}{R_p^2 + X_p^2}$$

$$Q = \frac{R_p}{X_p}$$

18.4 CIRCUITS EMPLOYING BIPOLAR TRANSISTORS

Figure:



(a) Transistor hybrid-pi model; (b) transformed version of the circuit in (a); (c) unilateralized circuit; (d) unilateralized circuit including loading on input and output due to R_3, C_3, R_n, and C_n.

The circuit of Fig. (a) is transformed to (b). The parameters are:

$$R_1 = r_{bb'} + r_{b'e}\left[\frac{r_{b'e} + r_{bb'}}{r_{b'e}+r_{bb'}+\omega^2(C_{b'e}+C_{b'c})^2(r_{bb'}r_{b'e}^2)}\right]$$

$$C_1 = C_{b'e} + C_{b'c} \Big/ \left[1 + \frac{r_{bb'}}{r_{b'e}} \right]^2 + \omega^2 r_{bb'}^2 \, (C_{b'e} + C_{b'c})^2$$

$$R_2 = \left[\frac{1}{r_{ce}} + \frac{1}{r_{b'c}} + g_m \frac{\frac{1}{r_{b'c}} \left(\frac{1}{r_{bb'}} + \frac{1}{r_{b'e}} \right) + \omega^2 C_{b'e} C_{b'c}}{\left(\frac{1}{r_{bb'}} + \frac{1}{r_{b'e}} \right)^2 + \omega^2 C_{b'e}^2} \right]^{-1}$$

$$C_2 = C_{b'c} \left[1 + \frac{g_m \left(\frac{1}{r_{bb'}} + \frac{1}{r_{b'e}} \right)}{\left(\frac{1}{r_{bb'}} + \frac{1}{r_{b'c}} \right)^2 + \omega^2 C_{b'e}^2} \right]$$

$$R_3 = r_{bb'} \left(1 + \frac{C_{b'e}}{C_{b'c}} \right) + \frac{1 + r_{bb'}/r_{b'e}}{r_{b'c} \cdot \omega^2 \cdot C_{b'c}^2}$$

$$C_3 = C_{b'c} \Big/ \left[1 + \frac{r_{bb'}}{r_{b'e}} - \frac{r_{bb'}}{r_{b'c}} \frac{C_{b'e}}{C_{b'c}} \right]$$

$$G_m = g_m \Big/ \sqrt{\left[1 + \frac{r_{bb'}}{r_{b'e}} \right]^2 + [r_{bb'} \cdot \omega (C_{b'e} + C_{b'c})]^2}$$

Ideally, the amplifier should be unilateral, i.e., it should be possible for a signal to be transmitted from the input to the output, but not vice versa.

A method for unilateralizing a transistor:

$I_f = -I_n$ (so that there is no net current leaving point b)

$$\frac{V_b - V_c}{R_3 + (1/j\omega C_3)} = - \frac{V_b - (-n \cdot v_c)}{R_n + (1/j\omega C_n)}$$

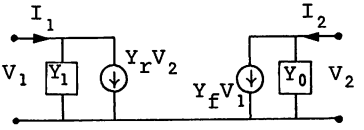
$$\frac{-V_c}{R_3 + (1/j\omega C_3)} \approx \frac{n \, v_c}{R_n + (1/j\omega C_n)}$$

$$R_n = n \cdot R_3 \quad \text{and} \quad C_n = \frac{C_3}{n}, \quad n = \frac{V_x}{V_c}$$

Once the circuit is unilateral, the input and output may be treated independently (Fig. d).

18.5 ANALYSIS USING ADMITTANCE PARAMETERS

The performance of an active device is predicted using Y-parameters, because these can be obtained at any specific frequency.

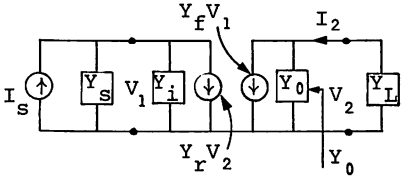


Using Y-parameters, because these can be obtained at any specific frequency.

$$Y_i = \frac{I_1}{V_1}\Big|_{V_2=0}, \quad Y_f = \frac{I_2}{V_1}\Big|_{V_1=0}$$

$$Y_r = \frac{I_1}{V_2}\Big|_{V_1=0}, \quad Y_o = \frac{I_2}{V_2}\Big|_{V_1=0}$$

A Y-parameter model with source and load added:



$$V_2 = -Y_f \cdot V_1 / Y_o + Y_L, \quad I_1 = (V_i \cdot Y_i) + \frac{-Y_f \cdot V_1}{Y_o + Y_L} \; Y_r$$

$$Y_i = \frac{I_1}{V_1} = Y_i - \left(\frac{Y_f \cdot Y_r}{Y_o + Y_L} \right)$$

$$V_1 = -V_2 \; Y_r / Y_i + Y_s, \quad I_2 = \frac{-Y_f \; V_2 \; Y_r}{Y_i + Y_s} + (Y_o \; V_2)$$

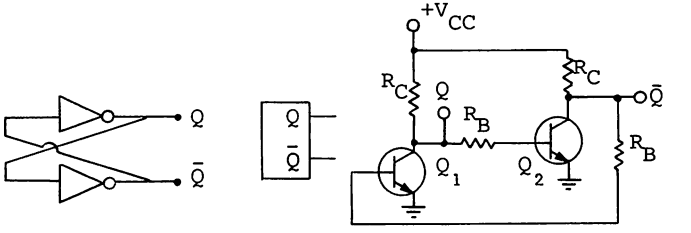
$$Y_o = Y_o - (Y_f \; Y_r / Y_i + Y_s)$$

CHAPTER 19

FLIP-FLOPS

19.1 TYPES OF FLIP-FLOPS

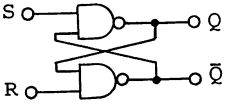
19.1.1 THE BASIC FLIP-FLOP



(c) Circuit implementation

The basic flip-flop simply consists of two RTL inverters.

19.1.2 R-S FLIP-FLOP

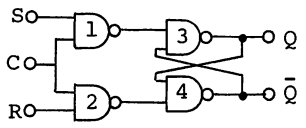


R	S	Q
1	1	unchanged
1	0	1
0	1	0
0	0	undefined

19.1.3 SYNCHRONOUS R-S FLIP-FLOP (CLOCKED R-S FLIP-FLOP)

The output state is set in synchronization with clock pulses.

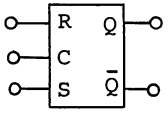
NAND-gate implementation:



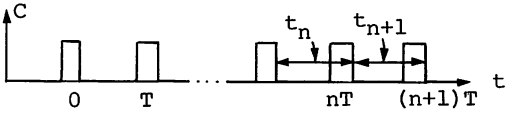
(a) Functional diagram

R_n	S_n	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	ND

(b) Truth table



(c) Symbol



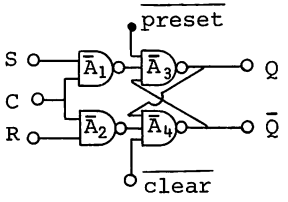
(d) Clock waveform

Gates 3 and 4 form an R-S latch with steering gates 1 and 2, used to input data to the device.

The clock is normally low, the outputs of gates 1 and 2 are then normally high and the state of the flip-flop cannot change. When C is high, the R and S inputs are steered to gates 3 and 4 and the flip-flop responds according to the truth table.

If R and S are low, the state of the flip-flop does not change, while Q in t_{n+1} is the same as it was in t_n, i.e., $Q_{n+1} = Q_n$.

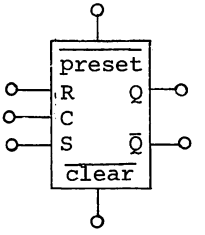
19.1.4 PRESET AND CLEAR



Synchronous		
R_n	S_n	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	ND
Asynchronous		
$\overline{clear}$	$\overline{preset}$	Q
0	1	0
1	0	1

(b) Truth table

General R-S Flip-Flop Signal Polarities
If S is high, Q=1
If R is high, Q=0
If $\overline{preset}$ is low, Q=1
If $\overline{clear}$ is low, Q=0



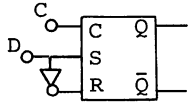
(c) Symbol

The two dc control lines are normally high.

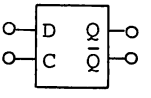
The functional diagram: The two dc control lines do not require the clockpulse and, in fact, override the clocked inputs.

The asynchronous or dc truth table holds for the dc $\overline{clear}$ and $\overline{preset}$ inputs.

19.1.5 D-TYPE FLIP-FLOP



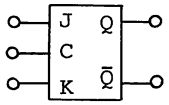
D_n	Q_{n+1}
1	1
0	0



(c) Symbol

With the D input connected to the S input and an inverter between R and S, the undefined output state that occurred in the R-S flip-flop is not possible here.

19.1.6 J-K FLIP-FLOP



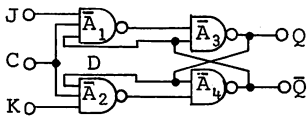
(a) Symbol

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

(b) Truth table

Q_n	Q_{n+1}	J_n	K_n
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

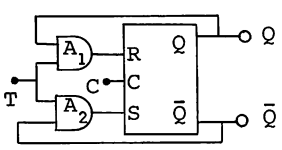
(c) Excitation table,
X = don't care



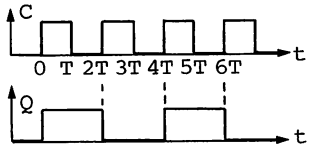
The J and K inputs listed in the truth table are the inputs present during time t_n. The output state is the flip-flop's state during t_{n+1} after a clock pulse at nT.

Excitation table: If the state Q_n of the flip-flop before clocking is known and the desired state Q_{n+1} after clocking is known, the necessary J and K inputs can be read from this table.

19.1.7 T-TYPE FLIP-FLOP

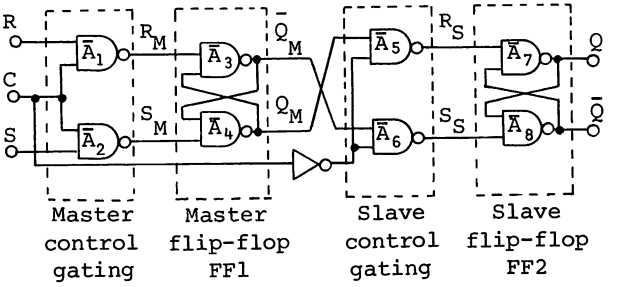


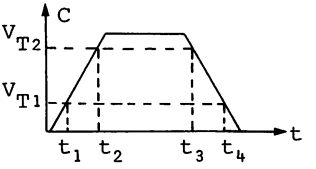
Functional Diagram



Waveforms when T=1

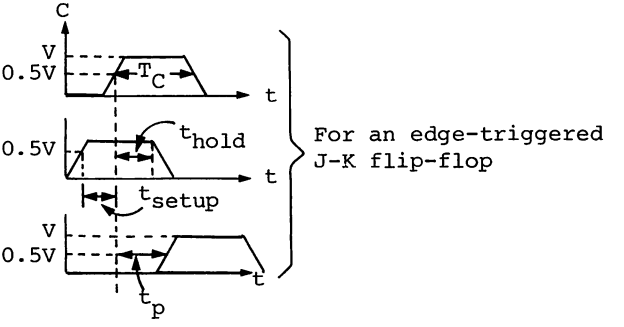
19.1.8 MASTER-SLAVE FLIP-FLOPS





Summary of Operations in the M-S Flip-Flop	
Time	Operation
t_1	disable slave from master
t_2	enable master (slave remains disabled)
t_3	disable master (slave remains disabled)
t_4	enable slave

19.2 FLIP-FLOP TIMING



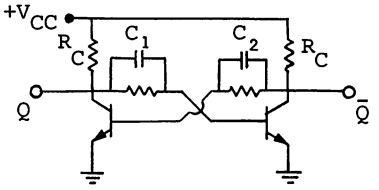
Hold, set-up and propagation time for a flip-flop:

The input data (J and K, R and S, or D) must be present and stable for some set-up time prior to the clock transition edge and for some hold time following the clock transition.

The clock transition edge is the rising edge of the clock pulse for a positive edge-triggered device and the falling edge of the clock pulse for a positive edge-triggered device.

Propagation time is measured from the 50% point on the clock transition edge to the 50% point on the output pulse edge.

19.3 COLLECTOR-COUPLED FLIP-FLOPS



Collector-coupled ff

Test Conditions for a Flip-Flop

1) Do two stable states exist, in each of which at least one transistor is not active?

2) Is the incremental loop gain, with all transistors active, greater than 1?

With Q_1 off, $I_{B_2} = (V_{CC}-V_{BES_2})/(R_C+R_B)$. If Q_2 saturates, $I_{C_2} = (V_{CC}-V_{CES_2})/R_C$.

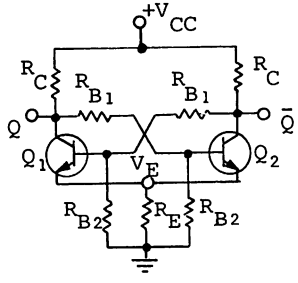
The condition for Q_2 to be saturated when Q_1 is off is:

$$I_{B_2} \approx (V_{CC}-V_{BES})/(R_C+R_B) \geq \frac{I_{C_2}}{\beta} = \frac{(V_{CC}-V_{CES})}{\beta \cdot R_C}$$

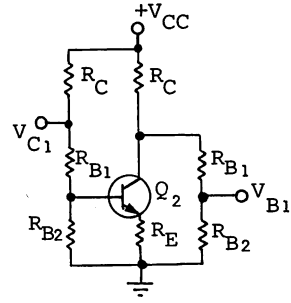
which is satisfied by any transistor with a minimum β,

$$\beta \geq \frac{V_{CC} - V_{CES}}{V_{CC} - V_{BES}} \cdot \frac{R_C + R_B}{R_C} \approx \frac{R_C + R_B}{R_C}$$

19.4 EMITTER-COUPLED FLIP-FLOPS



(a) Circuit



(b) Equivalent circuit, Q_1 off

With Q_1 off and Q_2 saturated, the emitter voltage is $V_E = (I_{B_2} + I_{C_2})R_E$. With Q_2 saturated, $V_{B_2} = V_E + V_{BES_2}$ and $V_{C_2} = V_E + V_{CES_2}$.

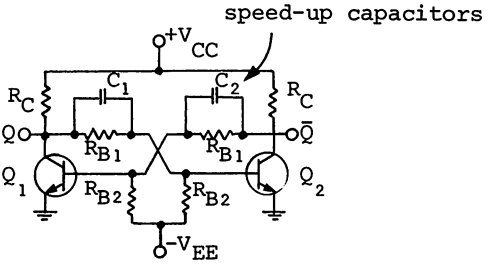
$$I_{C_2} = \left(\frac{V_{CC} - V_{C_2}}{R_C} + \frac{-V_{C_2}}{R_{B_1} + R_{B_2}} \right) \text{mA}$$

$$I_{B_2} = \frac{V_{CC} - V_{B_2}}{R_C + R_{B_1}} - \frac{V_{B_2}}{R_{B_2}}$$

Q_2 will saturate when Q_1 is off, if and only if $\beta \geq I_{C_2}/I_{B_2}$.

19.5 SWITCHING SPEED OF A FLIP-FLOP

Transition time: This is the time required for conduction to occur between two transistors. The transition time is reduced by using speed-up capacitors.



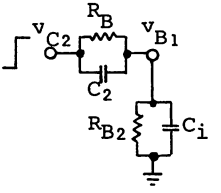
Fixed bias flip-flop

Without C_2 present, the input capacitance C_{i_1} is at the base of Q_1 will limit the time constant with which v_{B_1} can rise, and thus the rate at which Q_1 can turn on to:

$$[R_C \,||\, r_{sat_2} + R_{B_1} + (R_{B_2} \,||\, R_{i_1})]C_{i_1}$$

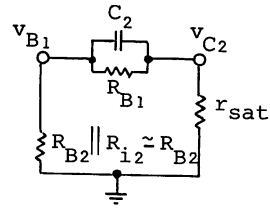
A model for Q_1 is turning on: The optimum value of C_2 for which v_{B_1} rises in zero time to its final value with no overshoot or undershoot is

$$C_2 = \frac{R_{B_2} \cdot C_{i_1}}{R_{B_1}}$$



(a) Compensated attenuator

Equivalent circuit with Q_1 off and Q_2 saturated:



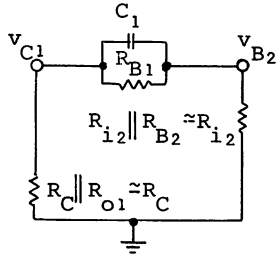
(b) Settling time for C

The voltage across C_2 changes at a rate

$$\tau_2 = [(R_{B_2}+r_{sat}) \| R_{B_1}]C_2,$$

$$\tau_2 \approx (R_{B_1} \| R_{B_2})C_2 \text{ [with } r_{sat} \text{ very small]}$$

Equivalent circuit for determining the recharging rate for C_1:



The value of the voltage on C_1 changes from its initial V_{C_2} value as soon as Q_1 has turned off. As Q_1 continues to be off, C_1 approaches its final steady-state value of

$$V_{C_2} = V_{C_1} - V_{B_2} \text{ at a rate } \tau_1 = [(R_{i_2}+R_c) \| R_{B_1}] \cdot C_1.$$

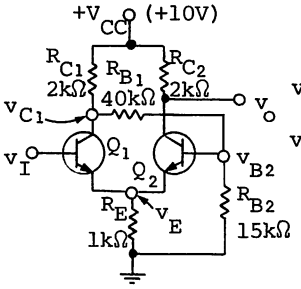
The settling time of the flip-flop: The time taken for C_1 and C_2 to recharge from their voltage levels ($V_{C_1} = V_{C_2} - V_{B_1}$ and $V_{C_2} = V_{C_1} - V_{B_2}$) to their new values ($V_{C_1} = V_{C_1} - V_{B_2}$ and $V_{C_2} = V_{C_2} - V_{B_1}$). (The values are interchanged.)

The resolution time is the sum of the transition time and the settling time. It is the total time the circuit requires to settle into its new steady state. It is a measure of the input trigger frequency that the circuit can resolve.

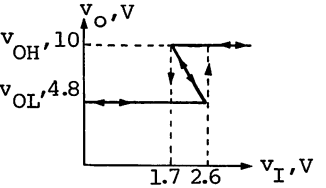
$$\text{The maximum frequency to which the flip-flop will respond} = \frac{1}{\text{The resolution time}}$$

19.6 REGENERATIVE CIRCUITS

Schmitt trigger:



Circuit



Transfer curve

Transfer curve:

The lower trace is the output response from V_I=0 to 2.6V. The maximum voltage for which Q_1 will remain off

$$V_{IL} = V_{B_2} = \frac{V_{CC} \cdot R_{B_2}}{R_{C_1} + R_{B_1} + R_{B_2}} = 2.6\text{v}.$$

While $V_I < \overline{V_{IL}}$, the output voltage is

$$V_o = V_{CC} - \frac{V_{B_2} \cdot R_{C_2}}{R_E} = V_{OL} \left(\text{where } I_{C_2} \approx I_{E_2} = \frac{V_E}{R_E} \approx \frac{V_{B_2}}{R_E} \right)$$

$$= 4.8\text{v}.$$

When Q_1 is ON and Q_2 is OFF, the nodal equation at v_{C_1} is

$$\frac{V_{CC} - v_{C_1}}{R_{C_1}} = i_{C_1} + \frac{v_{C_1}}{R_{B_1} + R_{B_2}}$$

The minimum $V_I = V_{IH}$ for which Q_1 shuts off occurs when $V_I = v_E = v_{B_2}$. With Q_1 on and Q_2 off,

$$v_{B_2} = \frac{v_{C_1} \cdot R_{B_2}}{R_{B_1} + R_{B_2}}$$

Hence,

$$v_{IH} = v_{B_2} = \frac{V_{CC}}{R_{C_1}} \left[\frac{1}{R_E} + \frac{1}{R_{B_2}} + \frac{R_{B_1} + R_{B_2}}{R_{B_2} \cdot R_{C_1}} \right] = 1.7\text{v}$$

For $v_I > v_{IH} = 1.7$, $V_o = V_{CC}$.

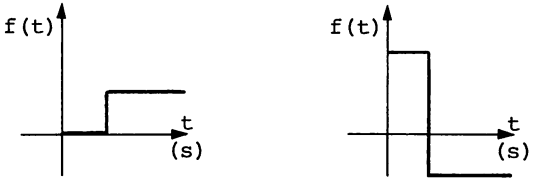
For inputs in the range $\overline{v_{IL}} = 2.6\text{V} > V_I > 1.7 = v_{IH}$, the output will be either high or low, depending on its prior time history.

CHAPTER 20

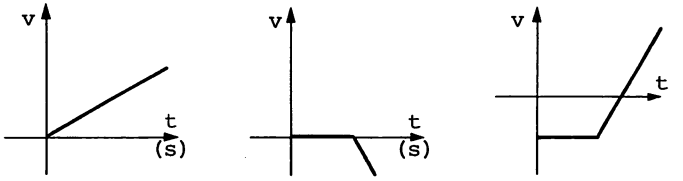
WAVESHAPING AND WAVEFORM GENERATORS

20.1 COMMON WAVEFORMS

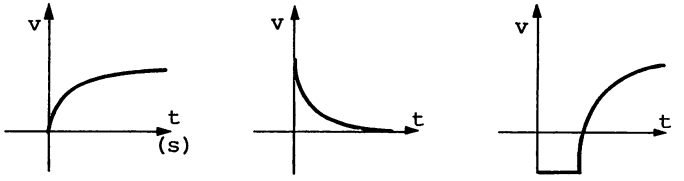
The step function: This function has an instantaneous change in level.



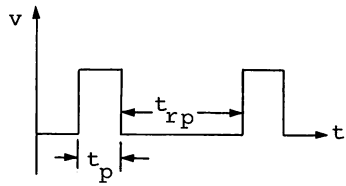
A ramp function:



The exponential function:



Pulse wave:



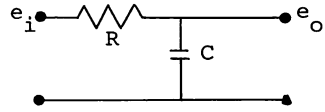
Pulse repetition time (PRT) = $t_p + t_{rp} = T$.

Pulse repetition rate (PRR) = $\frac{1}{T}$.

% duty cycle = $\frac{t_p}{PRT} \times 100\%$

20.2 LINEAR WAVESHAPING CIRCUITS

RC low-pass circuit:



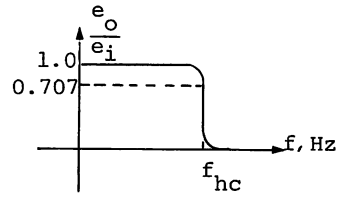
If the sinusoidal input e_i is applied, then

$$e_o = e_i \left(\frac{-jX_c}{R-jX_c} \right), \quad \text{where } X_c = \frac{1}{2\pi fc}$$

At low frequencies, $-jX_c >> R$, then $e_o \cong e_i$.

At high frequencies, $-jX_c << R$, then $e_o \cong 0$

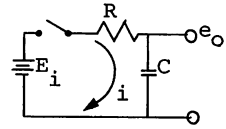
Frequency response:

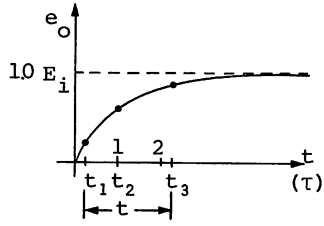


Cut-off frequency or half-power point frequency: The frequency at which the output (e_o) becomes 70.7 percent of the input e_i.

$$f_{nc} = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau}, \quad \tau = \text{Time constant of the filter}$$

Step input to an RC low-pass:





$$E_i = v_R + v_C = iR + v_C$$

$$= RC\frac{dv_c}{dt} + v_c$$

$$v_c = \text{The instantaneous voltage across C} = I_o R\left[1 - e^{-(t/\tau)}\right]$$

Curve characteristics:

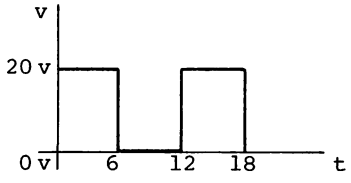
$t_o = 0$ and $v_c = 0$ $\quad t_3 = 2.3\tau$, $v_c = 0.9E_i$

$t_1 = 0.1\tau$, $v_c = 0.1E_i$ $\quad t_4 = 5\tau$, $\quad v_c \cong E_i$

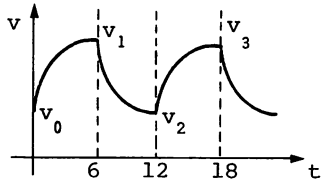
$t_2 = \tau$, $v_c = 0.632E_i$

t_r = The rise time = $t_3 - t_1 = 2.2\tau$

Pulse wave input to an RC low-pass:



Input waveform

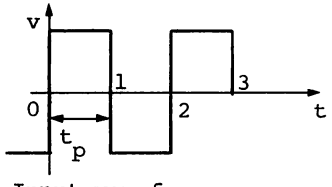


In steady state: $v_o = v_2$ and $v_1 = v_3$

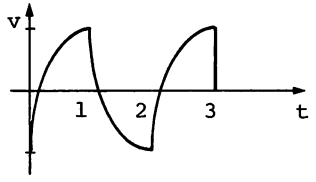
$$v_1 = E_i - (E_i - v_o)e^{-(t/\tau)}$$

$$v_2 = E_i - (E_i - v_1)e^{-(t/\tau)}$$

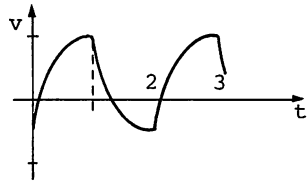
Effects of the circuit τ on the output waveform:



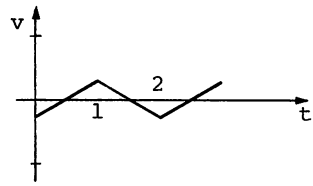
Input waveform



Short τ ($t_p > 10\tau$) circuit

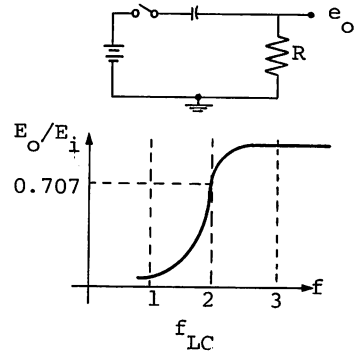


Medium τ ($10\tau < t_p > 0.1\tau$)



Long τ ($t_p < 0.1\tau$) circuit

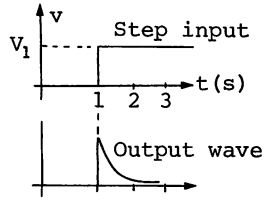
RC high-pass circuit:



$$e_o = \left(\frac{R}{R - jx_c} \right) e_i, \quad x_c = 1/2\pi f_c$$

Lower-cutoff frequency $f_{\ell c} = 1/2\pi RC = \frac{1}{2\pi} \cdot \frac{1}{\tau}$

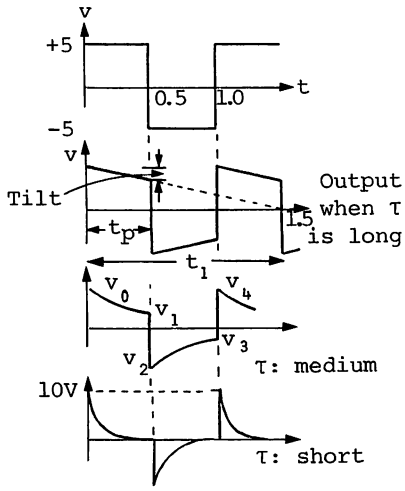
Pulse wave input:



$$v_R = E_i - v_c = (E_i \pm V_{ci})e^{-(t/\tau)}$$

$$v_R = E_o = E_i\, e^{-t/\tau} \quad (\text{for } V_{ci} = 0)$$

Effects of τ on the output waveform:



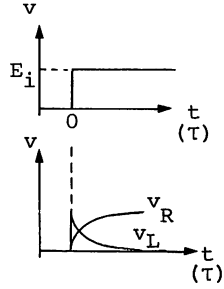
Fractional tilt $F_t = \frac{t_p}{t_t}$

(t_p = pulse width, t_t = Tilt time to reach 0 volt)

An R-C high pass circuit under short τ condition is called a differentiator.

RLC circuit:

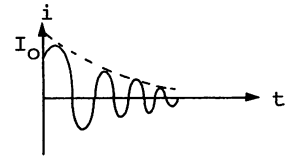
Step input to a series RL circuit:



$$v_R = E_i \left(1 - e^{\frac{-tR}{L}} \right)$$

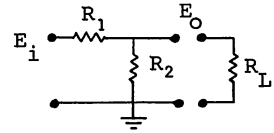
$$v_L = E_i \, e^{\frac{-tR}{L}}$$

Step input to a series RLC circuit:



Current in a underclamped circuit

Attenuators:

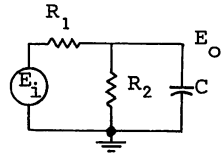


Simple attenuator

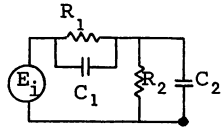
Attenuation factor: $\frac{E_i}{E_o} = \frac{R_2}{R_1+R_2}$

$$\frac{E_i}{E_o} \text{ (with } R_L) = \frac{R_2 \| R_L}{R_1+(R_2 \| R_L)}$$

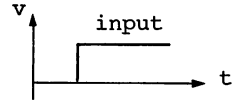
Uncompensated and compensated attenuator:

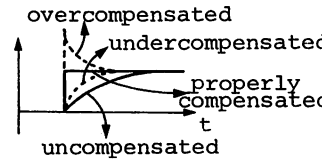


Uncompensated attenuator



Compensated attenuator





$$\frac{E_o}{E_i} = \text{Attenuation factor} = \frac{R_2 \| X_C}{R_1 + (R_2 \| X_C)}$$

$$\frac{E_o}{E_i} = \frac{Z_2}{Z_1 + Z_2}$$

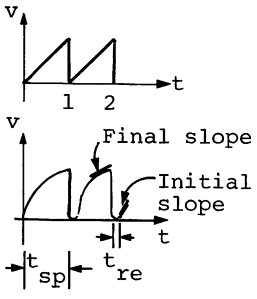
$$Z_1 = R_1 \| X_{c1} \quad \text{and} \quad Z_2 = R_2 \| X_{c2}$$

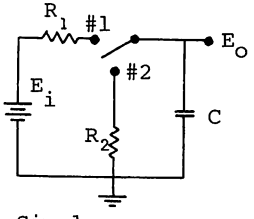
For proper compensation:

$$R_1 C_1 = R_2 C_2$$

20.3 SWEEP GENERATORS

Voltage sweep principles:





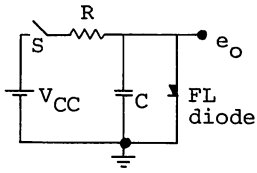
Simple sweep-generating circuit

t_{sp} = Sweep time, the time during which the function increases linearly.

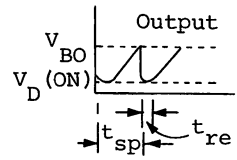
t_{re} = Retrace or flyback time, the time the function takes to drop back down to the initial base voltage.

$$\% \text{ slope error} = \frac{\text{Initial slope} - \text{final slope}}{\text{initial slope}} \times 100\%$$

Astable sweep circuit:



Four layer diode
sweep generator



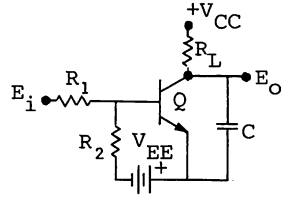
$$V_{BO} = \text{(Breakdown voltage)}$$
$$= V_{CC} - [V_{CC} - V_D(ON)]e^{-(t_{sp}/\tau_c)}$$

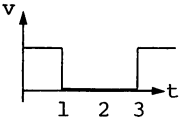
$$t_{sp} = \tau_c \cdot \ln \frac{V_{CC} - V_D(ON)}{V_{CC} - V_{BO}} \text{ (s)}$$

$V_D(ON)$ = Voltage across FL diode when it is on

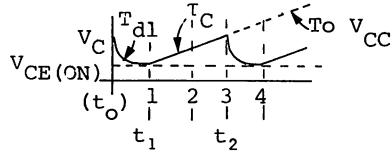
$\tau_C = RC$

Transistor sweep generator:





Input pulse waveform



V_C=voltage across capacitor just
before the transistor is ON

τ_C (charging time constant) = $R_L \cdot C$ seconds

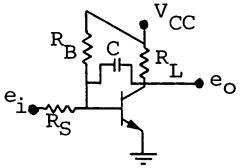
τ_d (discharge time constant) = $R_T \cdot C$ seconds

R_T = Equivalent resistance of the ON transistor = $\frac{V_{CE}(ON)}{I_C(ON)}$ ohms

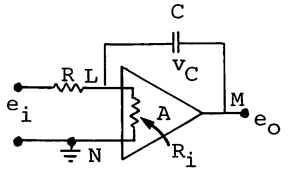
$$t_{sp} = t_2 - t_1 = \tau_c \cdot \ln\left[\frac{V_{CC}-V_{CE}(ON)}{V_{CC}-V_C}\right] \text{ seconds}$$

$$\text{Slope error} = \frac{V_C - V_{CE}(ON)}{V_{CC}-V_{CE}(ON)} \times 100$$

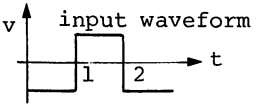
Miller sweep circuit:

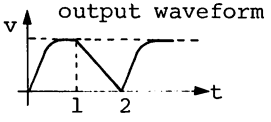


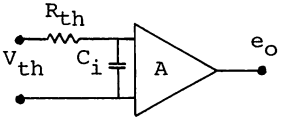
Practical Miller sweep



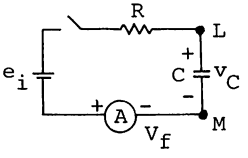
Miller integrator







Equivalent circuit



Basic circuit

Basic circuit: V_f is a fictitious voltage and is made such that its terminal voltage is always equal to the voltage across C but opposite in polarity. In such a case, a constant current E_i/R will flow n the circuit.

$$V_c = E_i \frac{t}{\tau} \text{ volts}$$

Miller integrator: This simulates the basic circuit.

Equivalent circuit:

$$C_i = C(1+A)$$

$$V_{th} = E_i(R_i/R+R_i)$$

$$R_{th} = R_iR/R_i+R$$

$$V_{ci} = V_{th} - V_{th} e^{-(t/R_{th} C_i)} \quad \text{... Capacitor charge equation.}$$

$$e_o = A \cdot e_i$$

$$= A \cdot V_{th} - A \cdot V_{th} e^{-(t/R_{th} C_i)}$$

The slope of the output for a high A:

$$A = \frac{e_o}{t} = \frac{E_i}{RC} = E_i \frac{t}{\tau_c}$$